Development of Back-Supportless CCD and Focal Plane Assembly for Soft X-ray Imager onboard the NeXT Satellite

Shin-ichiro Takagi
Department of Physics, Faculty of Science
Graduate School of Kyoto University

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Abstract

NeXT (New X-ray Telescope) is the next Japanese X-ray astronomy satellite, which is scheduled to be launched around 2010. Thanks to the included multilayer super mirror, *NeXT* has a large effective area in the 0.1–80 keV band. To detect all X-rays collected by the super mirror, the focal plane detector needs to be sensitive over a very wide energy band.

As the focal plane detector for *NeXT*, we have been developing a Wideband hybrid X-ray Imager (WXI) consisting of X-ray CCDs and a pixelized CdTe detector. The X-ray CCD of the WXI is required to maintain a high quantum efficiency up to the high energy band and pass hard X-rays undetected in the depletion (sensitive) layer.

In order to meet these requirements, we have invented, and have been developing a Back-Supportless CCD (BS-CCD) which has a thick depletion layer, a thinned Si wafer and a back supportless structure. As a first step, we manufactured a test model of the BS-CCD using an Nchannel CCD (Nch CCD). The Nch CCD was fabricated on a p-type silicon semiconductor, which is a standard type of CCD. The purpose of the trial production of the BS-CCD was to (1) investigate the handling and thinning process involved, and (2) confirm the absence of any change in the performance. From the view-point of mechanical strength and safe handling of the wafer, we decided to thin the wafer to ~ 200 μm thickness for the test model. We verified the thickness of the depletion layer and the wafer of the BS-CCD to be about 70 and 190 μm, respectively. The energy resolution at 5.9 keV of 144 eV and the read-out noise of 7 e^- are equal to those of the unthinned CCD, thus confirming that our thinning process has no effect on the performance. Based on these successful results, we constructed the "CCD-NeXT1" as an evaluation model of the BS-CCD. This device is a medium-sized CCD which can be loaded on to the satellite. The performance of this device is as excellent as those of test devices.

Through the development of the Nch BS-CCD, we found that (1) the thickness of the depletion layer is limited to 80–100 μm and (2) the thickness of the field-free layer is left 50–70 μm, as long as we adopt the Nch CCD. In order to remove the field-free layer completely, it is essential to increase the thickness of the depletion layer to > 150 μm. A promising device to realize such a thick depletion layer is the Pchannel CCD (Pch CCD), which is fabricated on an n-type silicon semiconductor.

We participated in the development of the Pch CCD, which was proceeded by a group of National Astronomical Observatory of Japan (NAOJ). We evaluated the performance of the Pch CCD, and were able to confirm that the thickness of the depletion layer reached over 300 μm. Furthermore, through our experiments to improve the performance, we were able to show that Pch CCD achieved excellent performance comparable to that of established X-ray CCDs .

In parallel to the development of a test device for the SXI, we also considered and designed a focal plane assembly (FPA). The FPA consists of a CCD chip, cold electronics of a thermal electric cooler (TEC), and associated electronics such as amplifiers and cables.

Since the CCD for the SXI will have a >4 times larger size than the X-ray CCD onboard the *Suzaku*, reducing the heat input to a CCD chip is inevitable in order to cool the CCD with low power consumption . We designed a new-type of TEC to match the unique structure of the SXI, and we also invented various schemes to reduce the heat input. Consequently, we were able to successfully reduce the heat input drastically and restrain the power consumption to cool the CCD.

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Chapter 1

Introduction

Observations in the hard X-ray band are very important in astronomy in order to explore the "non-thermal universe" characterized by accelerated high energy particles. The big breakthrough in X-ray astronomy was the discovery of non-thermal emission. Koyama et al., in 1995, discovered non-thermal X-ray emission from a supernova remnant SN 1006 using *ASCA* observations. This emission was considered to be synchrotron X-rays caused by high energy electrons on the order of 100 TeV. The distribution of such high energy electrons clearly departs from thermal equilibrium. This suggests that a portion of the particles is selectively accelerated and there is an unknown physics process which actively produces the nonequilibrium state.

After the discovery of non-thermal emission by Koyama et al., several supernova remnants (SNRs) emitting synchrotron X-rays were found. Furthermore, non-thermal X-ray emission has also been found in larger scale objects such as Galactic center, Galactic ridge, and clusters of galaxies in succession. These facts indicate that non-thermal X-ray emission occurs universally in celestial objects at various scales. Furthermore, the total amount of energy of non-thermal particles is estimated to be equal to that of thermal particles.

It is thus clear that non-thermal X-ray emission is a very important physical process for a comprehensive understanding of the universe. However, we still do not have a clear answer about its origin. One of the key reasons for this is that the thermal X-ray emission overwhelms the non-thermal emission in the energy band below 10 keV, where X-ray focusing optics so far have provided a high sensitivity in previous and current X-ray astronomy satellites. In order to reveal the nature of non-thermal X-ray emission, it is necessary to perform imaging and spectroscopic observations, and to investigate the spot from where the non-thermal X-rays are emitted. Because non-thermal emission becomes dominant in the energy regime above 10 keV, imaging and spectroscopic observations in this band are essential to solve the origins of the non-thermal emission.

The New X-ray Telescope (*NeXT*) satellite will be the next Japanese X-ray astronomy satellite following the *Suzaku*, and it is designed to carry out imaging and spectroscopic observations in the energy band above 10 keV. Thanks to new innovations including a multilayer super mirror, *NeXT* will be able to focus the X-rays in the energy range from 0.1 keV to 80 keV. In particular, this super mirror maintains a high reflectivity even in the high-energy ($>$ 10 keV) band. For the focal plane detector for *NeXT*, we have been developing a Wideband X-ray Imager (WXI). To match the wide energy range provided by HXT, we have combined (1) X-ray CCDs, which have excellent spatial and energy resolution, with (2) CdTe pixelized detectors, which have a high detection efficiency for X-rays and moderate spatial resolution. The former and the latter are respectively named the Soft X-ray Imager (SXI) and Hard X-ray Imager (HXI), based on the role played by each detector. X-ray CCDs are stacked above the CdTe detectors. The X-ray CCD performs precise imaging and spectroscopic observations in the energy band of 0.1–20 keV. On the other hand, since it is difficult to detect hard X-rays of above 20 keV by the CCD, we make them "penetrate" the CCD and enter the CdTe pixelized detector, which has sufficient sensitivity in the energy range up to 100 keV. The X-ray CCD is required to maintain a high detection efficiency to the high-energy band, while allowing hard X-rays to pass undetected through the depletion sensitive layer.

In order to realize the WXI and SXI, which are key to reveal the origins of non-thermal X-ray emission, we have been designing and developing a "back-supportless CCD" with a thick depletion layer, a thinned Si wafer and a back-supportless structure. In parallel, we have designed a focal plane assembly (a unit of a CCD and its cooling system) for the SXI, in order to cool the CCD chip with low power consumption, to the maximum extent possible.

In this thesis, in chapter 2, we first give a brief overview of the *NeXT* mission and the observation systems involved. In chapter 3, the principles and fundamental knowledge of the CCD are described. In addition, we give an outline of the data analysis method used which is peculiar to X-ray astronomy. In chapter 4, we describe the positioning of the SXI in the detectors onboard *NeXT* and development plans for the SXI. In chapter 5, we briefly introduce the experimental setup, which is used in the evaluation of the BS-CCD test device. In chapter 6, we state the results of the performance tests of the test devices for SXI and summarize the present status of the development of the BS-CCD. In chapter 7, we describe the design of the FPA for the SXI, especially focusing on the cooling system to cool a CCD chip efficiently on board the satellite.

Chapter 2

The *NeXT* mission

The *NeXT* (New X-ray Telescope) satellite is the next Japanese X-ray astronomy satellite mission after the *Suzaku* satellite and is slated to be launched around 2010. With the use of the multilayer super mirror (see [62] and references therein), *NeXT* has a large effective area for X-rays in the energy range from 0.5 to 80 keV. In particular, this super mirror can maintain a high reflectivity even in the high energy ($>$ 10 keV) band. In order to meet the energy range covered by the super mirror, we have developed a wideband camera which has high sensitivity in the energy band from sub-keV to $\sim$ 100 keV. Satellite missions with X-ray focusing optics in the energy band above 10 keV have never been realized thus far, and therefore, *NeXT* is expected to carry out imaging and spectroscopic observations in the energy band above 10 keV for the first time in human history.

2.1 Exploring the Nonthermal Universe - Key Science of *NeXT*

The *ASCA*, *Chandra*, *XMM-Newton* and *Suzaku* satellites have carried out precise imaging and spectroscopic observations mainly in the soft X-ray band ($<$ 10 keV) and have successfully discoverd many important phenomena. Though these observatories have detected non-thermal X-ray emission from many X-ray objects, the lack of sensitivity for X-rays over 10 keV have prevented us from confirming the nature of these emissions.

Since non-thermal emission, mainly due to accelerated high energy particles, dominates the thermal X-ray emission in the energy regime above 10 keV, observations of this band are essential to study the non-thermal X-ray emission. Therefore, the *NeXT* satellite is expected to open new windows to the “non-thermal universe”.

2.1.1 Non-thermal emission from supernova remnants (SNR)

The energy of a supernova explosion is mainly transformed into the energy of the ejected matter into interstellar space. Shortly after explosion, the ejected matter carries most of the explosion energy. The ejected matter thermalized by the interstellar medium and form plasma. In previous results, the thermal X-ray emission from high temperature thermal plasmas has been observed in the X-ray band. The picture that an SNR is a high temperature plasma sphere has been established as a general understanding for SNRs. However, *ASCA*, which is the 5th Japanese X-ray Astronomy satellite, has discovered non-thermal emission separate from the thermal emission in some young SNRs.

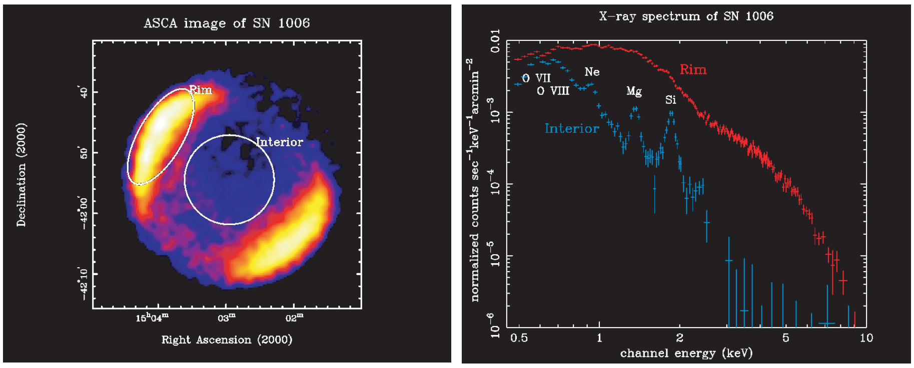


Figure 2.1: (left) The *ASCA* X-ray image of SN1006. X-ray spectra were obtained from two elliptical regions[33]. (right) The X-ray spectra from the rim and interior regions; the former is a non-thermal spectrum, while the latter is that of a thin thermal plasma typical of shell-like SNRs.

Figure 2.1 shows an X-ray image and spectra of the SN1006 SNR observed by the *ASCA* satellite. The X-ray spectrum from the interior region reveals a spectrum with many emission lines typically seen in a thermal plasma. However the spectrum from the rim of the SNR yields a featureless power-law spectrum. This represents non-thermal emission from the shell-type SNR. After this significant discovery, SNRs which show non-thermal emission have been discovered consistently in the hard X-ray band (see [70] and reference therein). The radiation mechanism is considered to be synchrotron emission by acceleration of high energy electrons. The electrons emitting synchrotron radiation at these X-ray energies must have energies on the order of 100 TeV [33].

Subsequently, the TeV gamma-ray telescope *Cangaroo* and *H.E.S.S* detected TeV gamma-rays in the SNR RXJ 1713.7−3946 and RXJ 0852−4622, which show nonthermal X-ray emission [1, 2, 3, 10, 28]. Although the origin of the TeV gamma-rays is still debatable, they found that the emission mechanism of the observed TeV gamma-rays is consistent with the inverse Compton scattering between relativistic electrons and photons of the cosmic microwave background (CMB). This may support the idea that the electrons are accelerated in an SNR, and then ions, including protons, are also accelerated. They are the main contributors to cosmic rays, and therefore the acceleration of charged particles in an SNR is a possible origin of cosmic rays.

However we have not fully understood the relationship between cosmic rays and the acceleration of charged particles in an SNR. Since it is difficult to obtain X-ray images in the energy band over 10 keV, we cannot observe the bending point of the non-thermal X-ray spectrum. X-ray observations so far have not determined with certainty how high energy an electron is being accelerated. Therefore we have not come to a definitive conclusion as to whether the origin of the highest energy cosmic rays is an SNR.

In addition, since nonthermal emission associated with SNRs has not been abundantly found so far, the question of what fraction of the (galactic) cosmic rays can be explained by SNRs has not yet been resolved.

To solve these problems, it is essential to perform imaging and spectroscopic observations in the hard X-ray band above 10 keV. Since $NeXT$ will have unprecedented high sensitivity for hard X-rays over 10 keV, we should be able to detect and study the bending point of the nonthermal spectrum. Furthermore, we can successfully separate nonthermal emission from thermal emission which dominates significantly and hides the nonthermal origin in the energy band below 10 keV. These results will be invaluable to solve the origin of cosmic rays.

We will also obtain the precise position-velocity map of expanding gas by the high-dispersion spectroscopic and imaging observations using the Soft X-ray Spectrometer onboard the $NeXT$ satellite. Based on this observation, we should be able to identify the place and the physical process associated with the energy conversion of the bulk motion to the thermal and nonthermal components.

2.1.2 Non-thermal emission from the Galactic center and Galactic ridge

$Tenma$ discovered strong X-ray emission from the hot plasma in the Galactic center (GC) and Galactic ridge (GR) regions. These X-ray spectra cannot be explained by one-temperature plasma and they have the nonthermal component extended to the gamma-ray band. The origins of the X-ray emission from the GC and GR remain unresolved. Since active star formation and supernova explosions occur in the Galactic plane, these activities may promote the acceleration of charged particles.

By the $NeXT$ observations in the hard (> 10 keV) X-ray band, we will be successfully able to separate nonthermal emission from the thermal emission diffused over the entire GC and GR, and obtain the spatial distribution and spectra of non thermal emission. Based on these results, we aim to resolve the spot and origin of the accelerated charged particles and the heating of the plasma.

2.1.3 Non-thermal emission from a cluster of galaxies

The *Einstein* satellite revealed large scale X-ray diffuse emission in the inter-galactic space of galaxy clusters [49]. The temperature of the diffuse plasma reaches $\sim 10^{7-8}$K and the total mass of the plasma is more than several times that of the optical galaxies. In order to bind such large-scale diffuse plasma with high temperature, the existence of dark matter is necessitated, and its mass should be more than several times that of the plasma.

The *ASCA* satellite first performed imaging and spectroscopic observations of clusters of galaxies in the wide energy band of 1–10 keV, and found a complex structure of the temperature. This suggests that the clusters have experienced collisions and mergers, and are not in an equilibrium condition. Since the clusters have an enormous kinetic energy of 10^{64}erg, a part of this energy may be used to accelerate charged particles via shock waves. In fact, spectra from several clusters contained a hard X-ray component in addition to diffuse thermal emission.

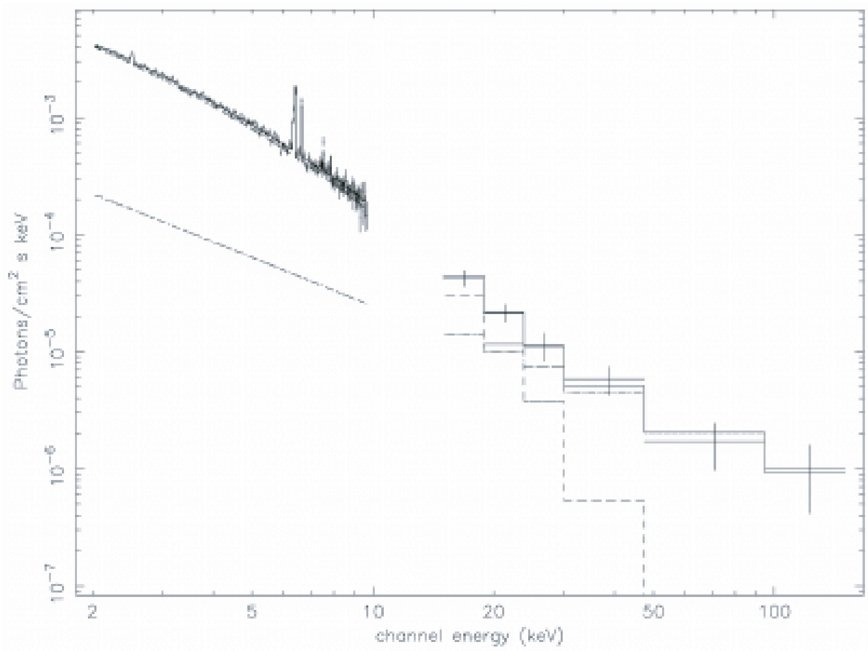


Figure 2.2: The *BeppoSAX* spectrum of the cluster of galaxies A2256 [13].

Figure 2.2 shows the spectrum of the A2256 cluster of galaxies [13] observed by *BeppoSAX*. In the energy band below 10 keV, thermal emission is observed by the CCD. On the other hand, the hard X-ray component, which shows a power-law spectrum, is dominated in the energy band of 10–100 keV. Though a plausible interpretation of the hard X-ray emission is inverse Compton emission by the non-thermal electrons and CMB photons[13], the origin has still not been definitively established.

Because this hard X-ray component will be distinguished clearly from the thermal emission in the energy band over 10 keV, the evidence of large-scale nonthermal emission will be obtained by further observations in the hard X-ray band. The hard X-ray (>10 keV) image, which will be obtained by $NeXT$ for the first time, will allow us to identify the location of the hard X-ray emission. In particular, if the inverse Compton emission is really the origin of this emission, the distribution and the spectrum of the hard X-ray emission will reveal the strength and distribution of the magnetic field in the clusters.

2.2 Overview of the Observation System

The observation system of $NeXT$ consists of the Hard X-ray Imaging System, Soft X-ray Imaging System, and a Soft Gamma-ray Detector. We show an overall view of the $NeXT$ satellite and its observation systems in Figure 2.3

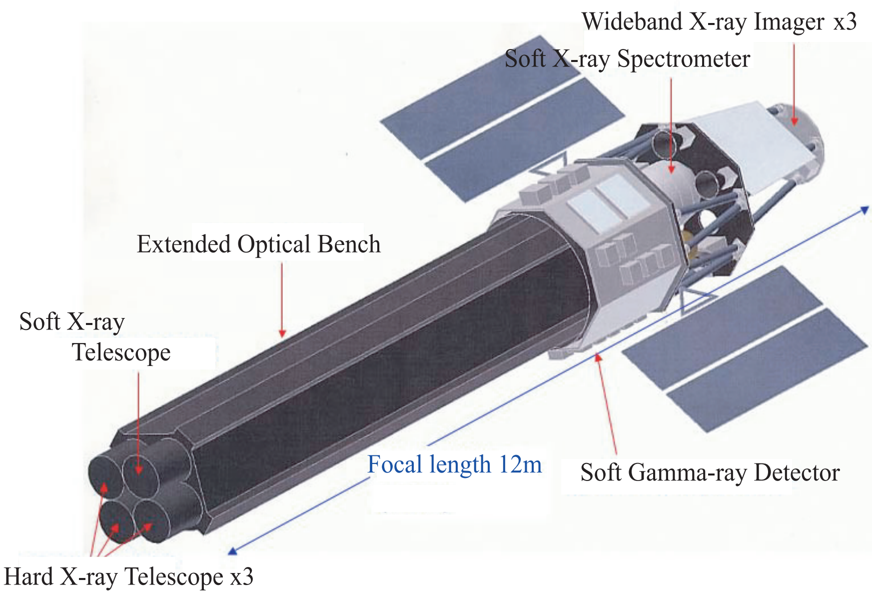


Figure 2.3: The overall view of the $NeXT$ satellite and its observation systems.

In this section, we briefly provide an overview of and explain the characteristics of each of the observation systems.

2.2.1 Hard X-ray Imaging System

Hard X-ray Telescope (HXT) In the X-ray band over 10 keV, satellites with X-ray focusing optics have never been available previously. Figure 2.4 shows the effective areas of various X-ray telescopes. In the case of present X-ray telescopes as *Chandra*, *XMM − Newton*, and *Suzaku*, the effective area declines rapidly in the energy band over 10 keV.

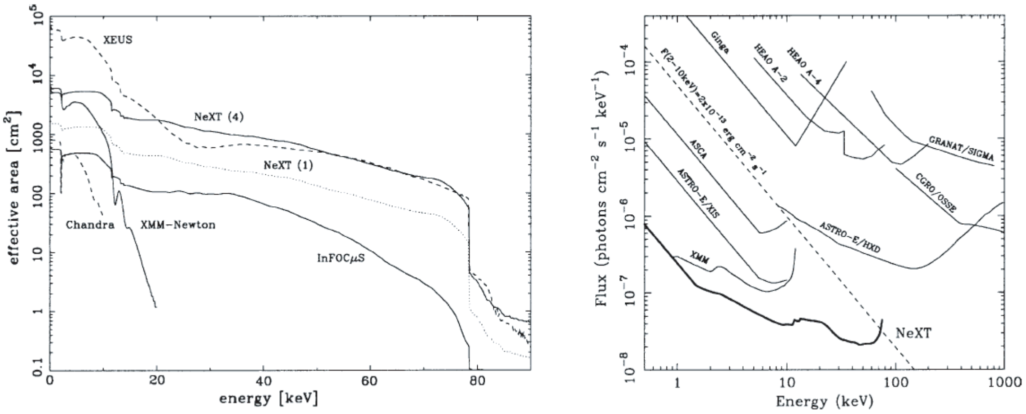


Figure 2.4: (left) Effective areas of the *NeXT* hard X-ray telescope, compared with the XMM-Newton, Chandra, InFOCμS and XEUS hard X-ray telescope.
(right) Limiting Sensitivities of various missions (right) with 5σ detection for a point-like sources. The NeXT X-ray telescope will achieve a sensitivity of 1.7×10^{13} erg cm^2 s^{-1} in the 10–80 keV region with a 100-ksec observation [50].

However, the **H**ard **X**-ray **T**elescope (**HXT**) onboard *NeXT* maintains a high effective area up to the X-ray energy of ~80 keV due to the "depth-graded multilayer" on its reflecting interface. This multilayer is a periodic structure which reflects X-rays by interference from the interfaces, similar to Bragg reflections from crystal lattice planes. Since its bandwidth is narrow and confined to close to the Bragg wavelength, the supermirror is a multilayer stack with different sets (blocks) of periodic lengths and number of layer pairs to cover different energy bands [74, 62, 50]. The multilayer is built up using platinum-carbon (Pt/C). From simulations performed by Okajima et al. (2004)[50], the effective area of NeXT is expected to be 250cm^2 per one HXT is 436, 210, and 73 cm^2, at 20, 40, and 60 keV, respectively. The rapid decline of the effective area at $\sim$ 80 keV is caused by the platinum K absorption line.

Wideband X-ray Imager(WXI) The focal plane detector for HXT is required to cover a very wide energy band from 0.1 to 80 keV. The standard focal plane detector is a CCD with excellent spatial and energy resolution. However, since the

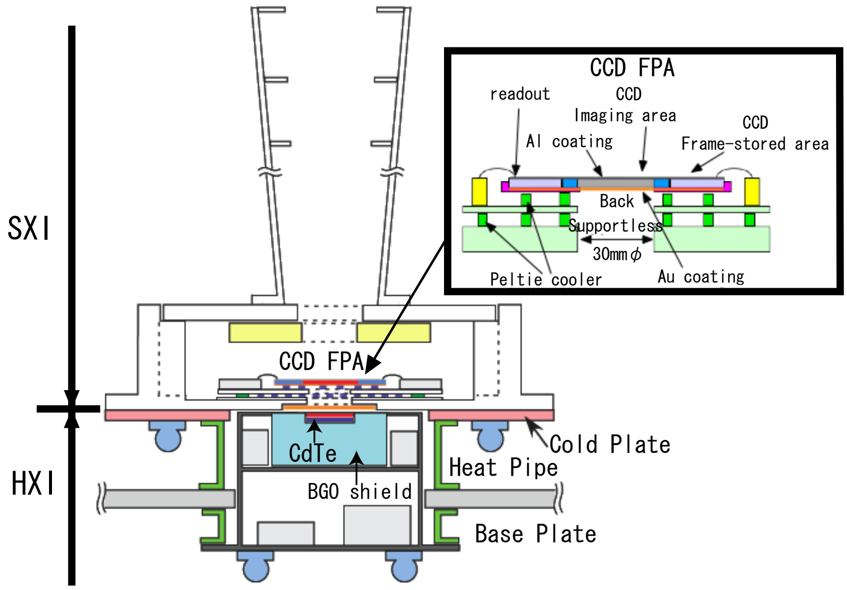


Figure 2.5: A schematic view of the Wideband X-ray Imager.

material of the CCD is silicon (low-atomic-number matter; low Z), the sensitivity for high energy X-rays is low. For example, the detection efficiency of the *Suzaku* XIS, which is one of the X-ray CCDs with the highest sensitivity, is limited to only ∼2% at 40 keV. On the contrary, the high Z solid detector has a high sensitivity at the high energy band with a moderate positional resolution. On the other hand, the spectroscopic and imaging performance of high Z solid detectors such as CdTe is poor below 10 keV compared to those of X-ray CCDs.

To compensate for the weak points of each other and to take advantage of both detectors, we have been developing the **W**ideband **X**-ray **I**mager (**WXI**) consisting of X-ray CCDs and CdTe pixel detectors[56, 57, 58, 67] placed under the X-ray CCDs. When the X-rays collected by the supermirror enter the WXI, the soft X-rays are detected by the CCDs and the hard X-rays, undetected by the CCD, penetrate the CCD and are detected by the CdTe detector. Therefore WXI enables us to carry out wideband imaging and spectroscopic observations together and is suitable for the focal plane detector of the HXT.

2.2.2 Soft Gamma-ray Detector

The **S**oft **G**amma-ray **D**etector has high sensitivity toward "soft Gamma-rays" which have an energy of a few × 10 keV – 1MeV. As shown in Figure 2.6(left), the SGD consists of a stack of 24 double-sided silicon strip detectors (DSSDs) and CdTe pixel detectors[58]. This structure allows the incident gamma-ray events to interacts twice in the detector. First, Compton scattering occurs in DSSDs, and secondoly, photo absorption of the scattered photon occurs in CdTe detectors. Based on the kinematics of the Compton scattering, the SGD can determine the arrival directions of detected gamma-rays within a cone in the sky (Compton ring). Thanks to the structure of a narrow field of view (FOV) using a well-type (phoswitch) active shield, the background events are efficiently rejected if the reconstructed Compton ring does not intercept the FOV[58].

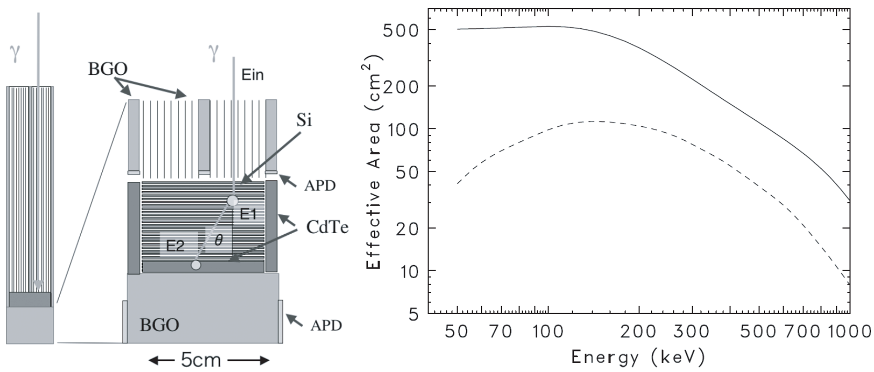


Figure 2.6: (left) A schematic view of the SGD[58]. A stack of 24 Si DSSDs and CdTe pixel detectors are assembled to form a semiconductor Compton Telescope. (right) Effective area of the SGD. The solid line shows the area calculated for the photo absorption mode. The dashed line shows the area when the detector is operated as a Compton camera (Compton mode) [59].

The right side in figure 2.6 shows the effective area of the SGD. The solid line shows the area when the detector is operated in the photo-absorption mode, which calculated only the energy of the incident gamma-rays. The effective area of the photo-absorption mode is greater than that of the Compton mode. However, the Compton mode improves the S/N ratio, especially for observations of faint objects, because this mode can determine the arrival direction of gamma-rays, as described above.

2.2.3 Soft X-ray Imaging System

Soft X-ray Spectrometer The **S**oft **X**-ray **S**pectrometer (SXS) adopts a TES(transition edge sensor)-type micro-calorimeter. An X-ray micro-calorimeter absorbs X-rays and produces signals proportional to the temperature rise induced by X-rays. The micro-calorimeter is usually operated at a low temperature (typically 0.1K), The TES is a very sensitive thermometer utilized by the rapid change of its resistance from the super conducting and normal states. The TES is thermally coupled to a cold bath whose temperature is below the transition temperature. When X-ray photon enters into the TES, the heat is generated and makes its state and resistance change. The heat rapidly moves the cold bath via a thermal link. Utilizing these characteristics, the aim for the SXS is to realize performance of (1) an energy resolution of 5 eV (at 5.9 keV), (2) a detector size of 12 mm $\times$ 12 mm, and (3) a format of 16 $\times$ 16pixels. Furthermore, a final goal is to achieve an energy resolution of 3 eV (at 5.9 keV) at a format of 32 $\times$ 32pixels.

2.2.4 Comparison of goal performance of each detector onboard *NeXT*

We summarize the performance goals of each detector onboard *NeXT* in Table 2.1.

Table 2.1: Goal performance of each detector onboard *NeXT* [47].

Hard X-ray Imaging System	HXT(Hard X-ray Telescope)		
		Effective area	500–1000 cm^2 (at 30 keV, HXT$\times$3)
		Energy band	0.5–60 keV
		Spatial resolution	30–40 arcmin
	WXI(Wideband X-ray Imager)		
	HXI(Hard X-ray Imager)		
		Energy band	0.5–60 keV
		Energy resolution	0.5–1 keV (FWHM)
		Pixel size	200–500 μm
		Detector size	20 mm $\times$ (20-30) mm
	SXI(Soft X-ray Imager)		
		Energy band	0.5–20 keV
		Energy resolution	130 eV (FWHM, 5.9 keV)
		Pixel size	27 μm
		Detector size	42mm $\times$ 43 mm (only imaging area)
Soft Gamma-ray Detector	SGD(Soft Gamma-ray Detector)		
		Energy band	10keV–1 MeV
		Energy resolution	2 keV (FWHM, 40 keV)
		Effective area	525 cm^2 (at 100 keV)
			110 cm^2 (at 500 keV)
			100 cm^2 (at 100 keV, Compton mode)
			40 cm^2 (at 500 keV, Compton mode)
		Spatial resolution	1.5 deg (RMS, Compton mode, 500 keV)
Soft X-ray Spectroscopic System	SXT (Soft X-ray Telescope)		
		Effective area	700 cm^2 (at 7 keV)
		Energy band	0.5–10 keV
		Spatial resolution	30–40 arcmin
	SXS (Soft X-ray Spectrometer)		
		Energy b and	0.5–10 keV
		Energy resolution	2–5 eV (FWHM, 7 keV)
		Effective area	525 cm^2 (at 100 keV)
		Pixel size	>12 mm
		Format	12 $\times$ 12 – 32 $\times$ 32 pixels

Chapter 3

Charge-Coupled Device

In 1969, a charge coupled device (CCD) was invented by W. S. Boyle and G. E. Smith at Bell Telephone Laboratories[7]. Though they originally developed it as a memory device, M. F. Tompsett at Bell Telephone Laboratories suggested the idea in 1971 of using the CCD as an imaging device. W. J. Bertram et al. (1972) and C. H. Séquin et al. (1973) successfully developed CCDs of 98 pixels [6] and $106 \times 128 = 13568$ pixels[53], respectively. After the CCD gained recognition as a new 2-dimensional imaging area sensor, its development progressed rapidly. Based on the progress of semiconductor processing, the number of pixels was eventually increased to over 10^6 pixels, and the CCD became one of the most representative and popular detectors among imaging devices.

Today, CCDs are widely used in various applications including commercial, industrial, and scientific. In astronomy, CCDs are also widely employed, especially in optical, infrared, and X-ray astronomy. Since the sensitivity of a CCD is significantly higher than that of a film[24] for photons in the 300–1000 nm-wavelength range, and a CCD has the moderate time resolution, most optical astronomical observatories employ a CCD as a focal plane detector instead of films.

The CCD has also become a standard detector for X-ray astronomy, with an energy resolution of $\sim$ 130 eV at 5.9 keV (FWHM), position resolution reaching $\sim 20\mu$m, time resolution of several seconds, and sufficient detection efficiency in the 0.1–10 keV band. An X-ray CCD as the focal plane detector for X-ray astronomy mission was first used in the *ASCA* satellite launched in 1993. Since then, X-ray CCDs have become standard focal plane detectors. The new generation of X-ray observatories, including *Chandra*(1999-), *XMM-Newton*(1999-) and *Suzaku*(2005-), are all equipped with CCDs as the focal plane detectors. Table 3.1 shows the performance of representative X-ray CCDs onboard various X-ray astronomy satellites [8, 61, 54, 69, 71].

Table 3.1: Comparison of Various X-ray CCDs

Observatory	*ASCA*	*Chandra*	*XMM − Newton*		*Suzaku*
Detector	SIS	ACIS	EPIC-MOS	EPIC-PN	XIS
Year	1993–2000	1999–	1999–		2005–
Country	Japan	USA	ESA		Japan
Pixel size [μm]	27	24	40	150	24
Energy resolution [eV]†	~130	~130	~130	~130	~130
Depletion depth [μm]	35	70	35	280	70(FI)/45(BI)
Type	MOS	MOS	MOS	PN	MOS

†: Energy resolution of the 5.9 keV line (FWHM).

3.1 Physical Structure of the CCD

3.1.1 MOS capacitor

The fundamental building block of a CCD is the MOS capacitor. This element is the backbone for charge collection and charge transfer. We show a cross-sectional view of a CCD in Figure 3.1. In the following, we assume that a MOS capacitor consists of a p-type silicon semiconductor. A silicon semiconductor is oxidized to form an insulator (SiO_2), and a poly-Si electrode is deposited as a gate structure to form a MOS capacitor.

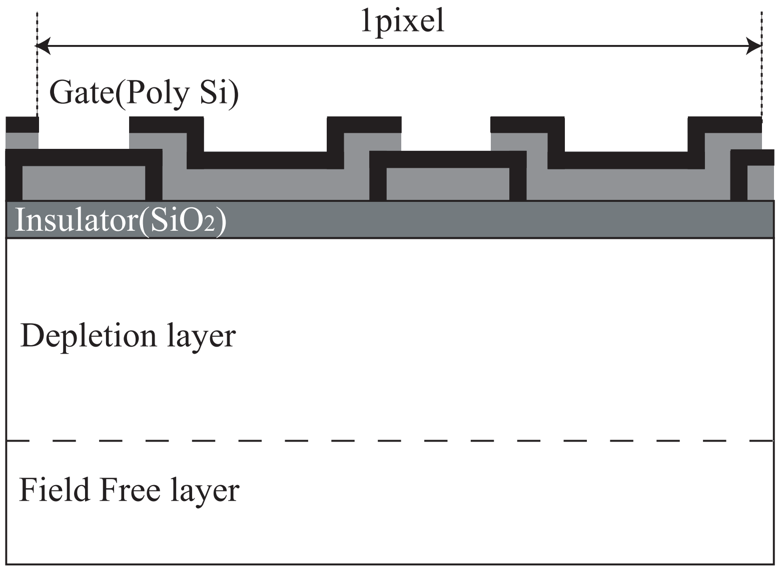


Figure 3.1: A schematic view of a MOS CCD

A positive voltage applied to the gate forms a depletion layer, wherein majority carriers (holes in the case of a p-type semiconductor) are driven out from the surface.

Uncompensated, negatively charged acceptors were left in the depletion layer. Then, the biased distribution of the charge prevents further drift of carriers and makes the bias condition in equilibrium, as shown in Figure 3.2(left). The potential is plotted as a function of depth in the silicon. Below the depletion layer, there is a region called the "field-free region", where forms little electric field condition.

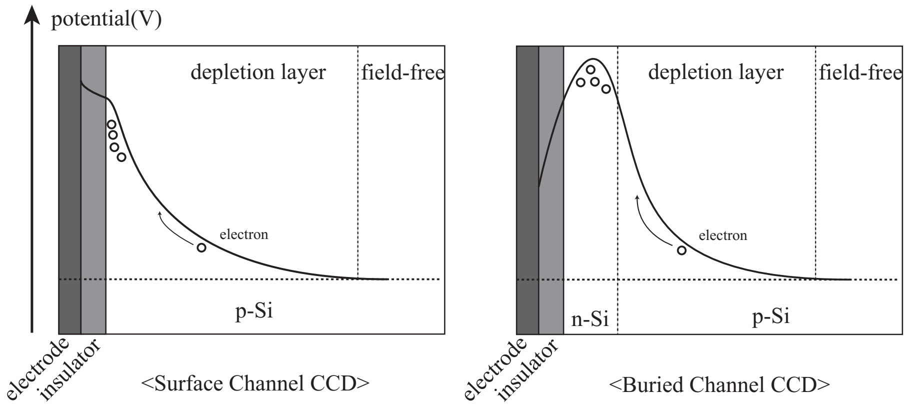


Figure 3.2: A schematic view of a potential well, in the case of surface channel CCD (left), and in the case of buried channel CCD (right).

When an X-ray photon is injected onto a CCD, it is absorbed by a Si atom via photoelectric absorption. A hot electron is then emitted which collides with another atom, multiplying the number of electrons. These are pulled up to the CCD surface by the electric field in the depletion layer. It is basically difficult for the charges generated in the field-free region to reach the CCD surface, since there is little electric field in this region. Therefore, we usually call the depletion layer and the field-free layer as the "sensitive" and "dead" layers, respectively. The sensitivity of the X-rays depends on the thickness of the depletion layer. We can derive the equation of the thickness of the depletion layer, as shown in the following step [24];

In the whole of the depletion layer, the number of holes driven out from the surface equals the number of negative charges on the surface of a CCD (in other words, the electrode),

$$Q_s = -qN_A x_d, \tag{3.1}$$

where Q_s is the ionized acceptor charge concentration beneath the depleted MOS electrode, N_A is the acceptor doping concentration, x_d is the thickness of the depletion layer, and q is the elementary electric charge.

Then, a potential voltage $\phi(x)$ is generated from the surface to the depletion layer. $\phi(x)$ is found by solving the following Poisson's differential equation,

$$\frac{\partial^2(\epsilon_{Si}\epsilon_0\phi(x))}{\partial x^2} = qN_A, \tag{3.2}$$

where x is the depth measured from the surface, ϵ_{Si} is the relative permittivity of silicon, and ϵ_0 is the permissivity of free space.

Assuming the following boundary conditions;

- the electric field is equal to zero at $x = x_d$, or

$$\frac{\partial(\epsilon_{Si}\epsilon_0\phi(x_d))}{\partial x} = 0, \tag{3.3}$$

- the potential is zero (reference potential) at $x = x_d$, or

$$\phi(x_d) = 0, \tag{3.4}$$

then we can solve Eq. (3.2) as follows;

$$\phi(x) = \frac{-qN_D(x - x_d)^2}{2\epsilon_{Si}\epsilon_0}. \tag{3.5}$$

Assuming that the potential voltage of the surface of the CCD is ϕ_s, we can solve the thickness of the depletion layer as:

$$x_d = \sqrt{\frac{2\epsilon_{Si}\epsilon_0\phi_s}{qN_A}} \tag{3.6}$$

It can be seen that the thickness of the depletion layer increases by the square root of the surface potential voltage ϕ_s and decreases with the square root of the doping concentration N_A. We can simplify the above equation to:

$$x_d \propto \sqrt{\frac{\phi_s}{N_A}}. \tag{3.7}$$

In the case of the p-type semiconductor, the resistivity of the semiconductor $\rho_{\text{p-type}}$ and impurity concentration N_A is related as:

$$\rho_{\text{p-type}} = \frac{1}{\mu_p N_A}, \tag{3.8}$$

where μ_p is the mobility of holes, which is the major carrier in a p-type semiconductor.

By combining Eq. (3.7) and (3.8), the relationship for the depletion depth ($x_{d,\text{Nch}}$) for a p-type semiconductor is given by:

$$x_{d,\text{Nch}} = C\sqrt{\mu_p \rho_{\text{p-type}} \phi_s}. \tag{3.9}$$

In the same way, the thickness of the depletion layer ($x_{d,\text{Pch}}$) for an n-type semiconductor equals:

$$x_{d,\text{Pch}} = C\sqrt{\mu_n \rho_{\text{n-type}} \phi_s}, \tag{3.10}$$

where $\rho_{\mathrm{n-type}} and\ \mu_n$ are the resistivity of an n-type semiconductor and the mobility of electrons, which is the major carrier of an n-type semiconductor, respectively. C is the common constant in the above two equations. It can be clearly seen that the thickness of the depletion layer significantly depends on the resistivity of a semiconductor and the gate voltage. In general, the relationship for the thickness of the depletion layer is given by:

$$x_d \propto \sqrt{\mu \rho \phi_s}, \tag{3.11}$$

where $\mu,\ \rho$ represent the mobility of the major carrier and the resistivity of a semiconductor, respectively.

3.1.2 Surface-Channel and Buried-Channel CCD

As the model considered in the above calculation, a CCD consisting of a silicon semiconductor (p-type Si), an insulator (SiO_2), and a gate electrode (poly-Si) has the potential well at the interface of the Si-SiO_2 (see also Figure 3.2 (left)). Therefore the generated charge is stored and transferred along the surface of the semiconductor. We call the CCD with such a potential structure as a surface-channel CCD. Since the structure of the surface-channel CCD is very simple, earlier CCDs were formed with this structure. However, there is a major problem associated with surface-channel CCDs. Since there are many trap levels at the Si-SiO_2 interface, signal charges transferred near the interface are often trapped and this makes the performance of charge transfer inefficiency (CTI) severely worse.

To avoid this surface-state problem, the "buried-channel CCD" was invented. As shown in Figure 3.2 (right), a thin doped n-type Si region is formed between the insulator and p-type Si. Then, the potential well is formed in the n-type Si layer.

Since the generated charges are stored and transferred in the potential well which lies beneath the surface, they are free from the trap levels present at the surface. In contrast to the surface-channel CCD, the CTI performance for the buried-channel CCD is remarkably high. Today, most CCDs are equipped with a buried channel, including the CCDs described in this thesis.

3.1.3 Front illuminated and Back illuminated CCD

CCDs are classified into two types, "front-illuminated CCD" (FI-CCD) and "back-illuminated CCD" (BI-CCD). In the FI-CCD, the photons enter the CCD from the electrode side. Though the surface electrode and insulator are very thin, the absorption of soft X-rays below 1 keV is not negligible. Figure 3.3 shows the properties of the transmission of the surface electrode (poly-Si) and insulator (SiO_2). The thickness is assumed to be 0.45 μm for the poly-Si and 0.35 μm for the SiO_2, which are the nominal value for the FI-CCD onboard the *Suzaku* satellite (XIS-FI). We can clearly see soft X-rays below 1 keV are significantly absorbed.

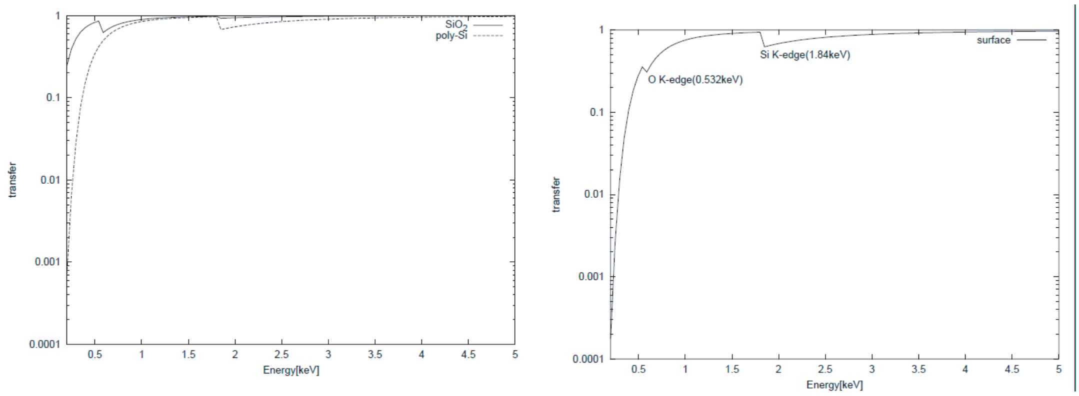


Figure 3.3: (left) Transmission of the surface electrode (poly-Si) and insulator (SiO_2). The former and latter are shown by the dotted and solid curves, respectively. (right) Total transmission of the surface of XIS-FI.

In the case of the BI-CCD, the field-free region, which is virtually insensitive for photons, is removed. Since photons directly enter the depletion layer, the sensitivity for soft X-ray photons is improved compared with the FI-CCD. Figure 3.4 shows a comparison of the sensitivity for X-rays of XIS-FI and XIS-BI (back-illuminated CCD onboard the *Suzaku* satellite). It can be seen that the sensitivity of the XIS-BI for soft X-rays below 1 keV is higher than that of the XIS-FI [5].

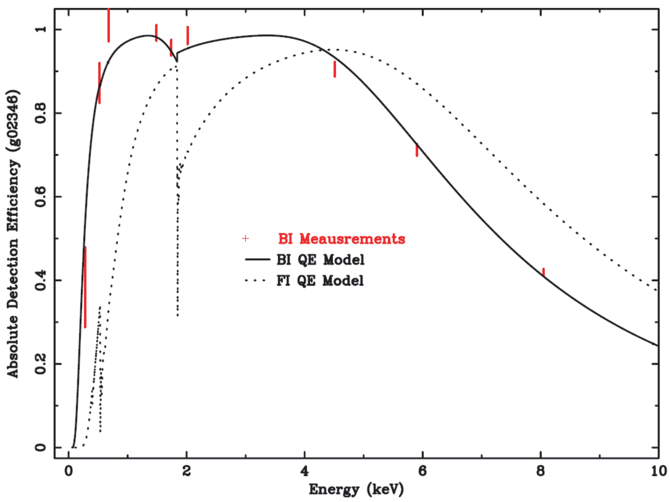


Figure 3.4: Comparison of the sensitivities of XIS-FI (dotted curve) and XIS-BI (solid curve) [5].

3.2 Charge Transfer

A CCD is a monolithic array of closely spaced MOS capacitors that transfers an analog signal charge from one pixel to another, working as an analog shift register. In this section, we describe the principle and mechanism of charge transfer in a CCD.

3.2.1 Principle of Charge Transfer

The charge stored within a pixel is transferred from pixel to pixel, and is measured via a readout node. Combining the horizontal transfer and vertical transfer, we can obtain information on all pixels arranged in a 2-dimensional array with only one readout node. To help in our understanding, we show the simplest and an understandable analogy for the operation of the CCD in Figure 3.5 [23, 24];

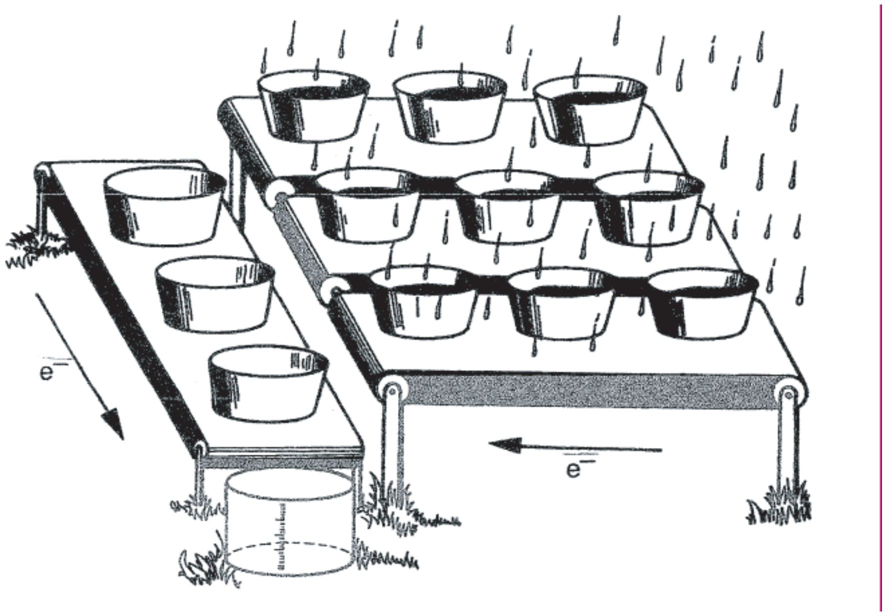


Figure 3.5: Bucket analogy used to describe CCD operation [23, 24].

In a CCD, the transfer of charge is carried out by manipulating the voltage applied to the gate electrode, instead of the belt conveyor in the bucket analogy. We change the voltage periodically and form potential slopes in order to transfer the charges. There are two methods for forming the potential slopes;

- **Multiple transfer electrodes**

  A few transfer electrodes are deposited on each pixel. Applying voltage to each electrode independently, we can form a potential slope as needed. Though the pattern of the voltage is complex, there is little restriction in the way of charge transfer.

- **Additional dopant**

  We dope impurities non-uniformly on each pixel to form a natural potential slope. The number of electrodes in this case is reduced, and it simplifies the pattern of the voltage. However, the charge transfer is limited to one direction, which is determined by the spatial distribution of the additional dopant.

All the CCDs developed in this work and described in this thesis employ the "**two phase transfer method**", which is a combination of the above two methods. We show the scheme of the two phase transfer method in Figure 3.6.

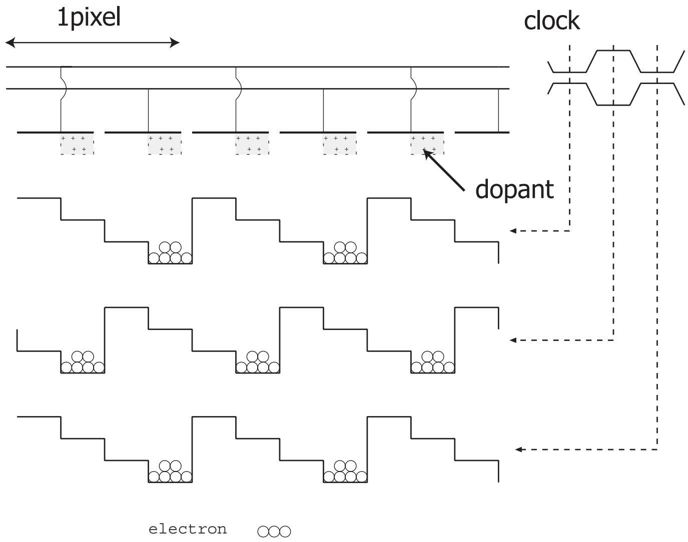


Figure 3.6: Schematic view of the 2-phase transfer method.

Two electrodes are deposited on each pixel, and applied arbitrary voltages can be applied independently to each of the two. Furthermore, an additional impurity is doped on the half side of each pixel. By applying the pattern of voltages (clock pattern) shown in Figure 3.6 to each pixel, the periodic change in the potential well in a CCD transfers the signal charges.

For comparison, we also describe the other methods of charge transfer;

- **Virtual phase transfer**

  As shown in Figure 3.7(left), a single electrode, which is half the size of a pixel, is deposited on each pixel [22, 20]. The applied voltage is strikingly limited because the voltage potential of the other half side of the pixel is fixed. However, by leaving half the pixel open, this method allows photons to enter this open area without significant absorption by the electrode. The sensitivity to photons which cannot penetrate the electrode significantly is thus improved.

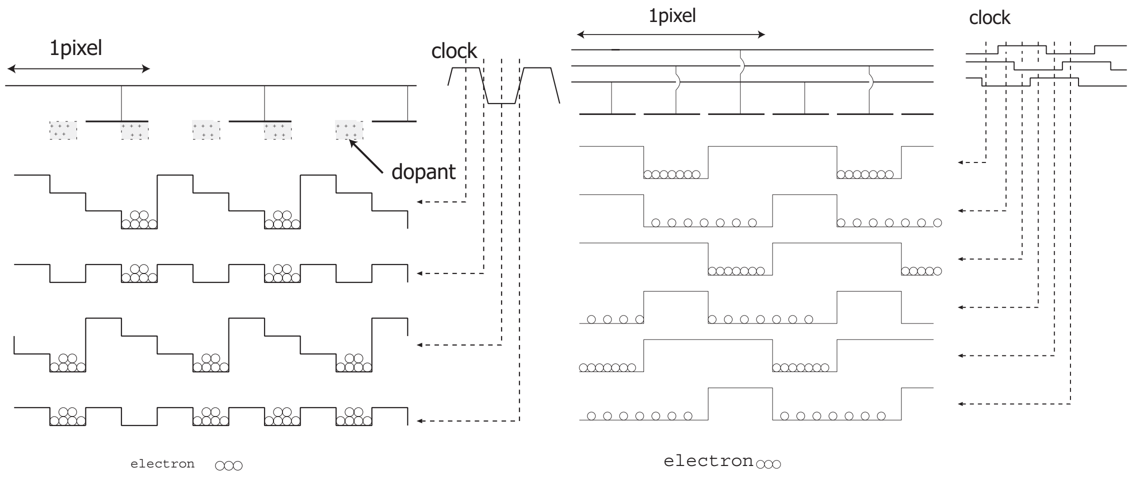


Figure 3.7: Schematic views of the virtual phase (left) and 3-phase (right) transfer methods.

- **Three-phase transfer**

  As shown in Figure 3.7(right), in this method, three electrodes are deposited on each pixel. Any additional impurity doping is unnecessary, allowing us to freely select the direction of transfer by applying suitable clock patterns. Thus, this method allows for bi-directional charge transfer.

3.2.2 Scheme of Charge Transfer

CCDs can be classified into 3 types based on the difference in the scheme of the charge transfer; frame transfer CCD (FT CCD), full frame transfer CCD (FFT CCD), and interline transfer CCD (IT-CCD). A schematic view of each type of CCD is shown in Figure 3.8. In this subsection, we describe the scheme of charge transfer and characteristics of each type of CCD.

1. Frame Transfer CCD (FT CCD)

   The FT CCD consists of an imaging area (IA) exposed to incoming light and a frame stored region (FS) shielded from light. At the end of the exposure, the charges acquired in the IA are quickly transferred to the FS. During the readout of the charges transferred to the FS, new exposure can proceed on the IA. Therefore the dead time due to the readout time is significantly reduced by adopting this transfer scheme. Furthermore, because the charges in the IA are transferred in a short time, a mechanical shutter to shield the incoming light in the transfer phase is unnecessary, in general. However, approximately half of the CCD is shielded in the FS region, and therefore the effective area is smaller than that of other CCD types.

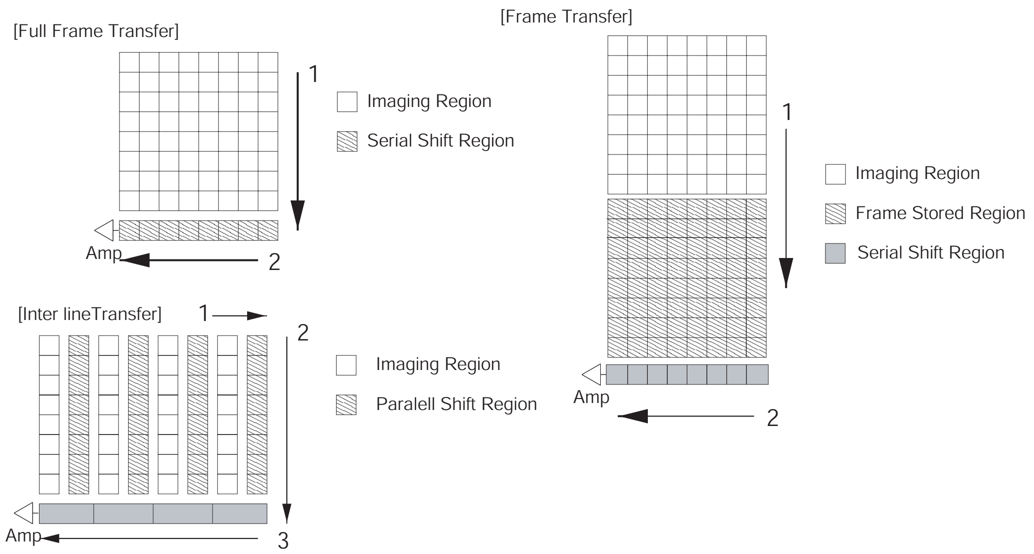


Figure 3.8: The scheme of charge transfer in (upper left) full frame transfer CCD, (right) frame transfer CCD, and (lower left) interline transfer CCD.

2. Interline Transfer CCD (IT CCD)

   The IT CCD is a spatially constructed device in which each column of the imaging (active) pixels is paralleled by a light-shielded (inactive) column of storage [19]. At the end of the exposure, charges stored in each active column are quickly shifted to its neighboring light shielded column. The shift occurs in a very short time (only 1 time transfer!), and therefore, a mechanical shutter is unnecessary. The shifted charges can be transferred to a readout node while the active columns are newly exposed.

   However, the IT CCD is rarely employed for X-ray use. This is because the X-ray photons easily penetrate the aluminum coating which is usually too thin to absorb the X-ray photons.

3. Full Frame Transfer CCD (FFT CCD)

   In this case, the whole area of a CCD is an IA. Compared to the FT CCD and IT CCD, there is no dead area. However, during the transfer phase, the FFT-CCD needs to be shielded against incoming photons with the use of a mechanical shutter.

Most of the CCDs developed in this study and described in this thesis employ the FFT-CCD method except as noted. Only the “CCD-NeXT1” device is classified as an FT-CCD (see chapter 6).

3.3 Charge Measurement

3.3.1 Structure of Output Amplifier

The charges are transferred to a readout node using one of the above methods and then finally converted to a voltage which corresponds to the amount of charges stored in each pixel. A typical example of a readout node of a CCD sensor is an output with a floating diffusion layer, termed the ”floating diffusion amplifier (FDA)” We show a schematic view of FDA in Figure 3.9.

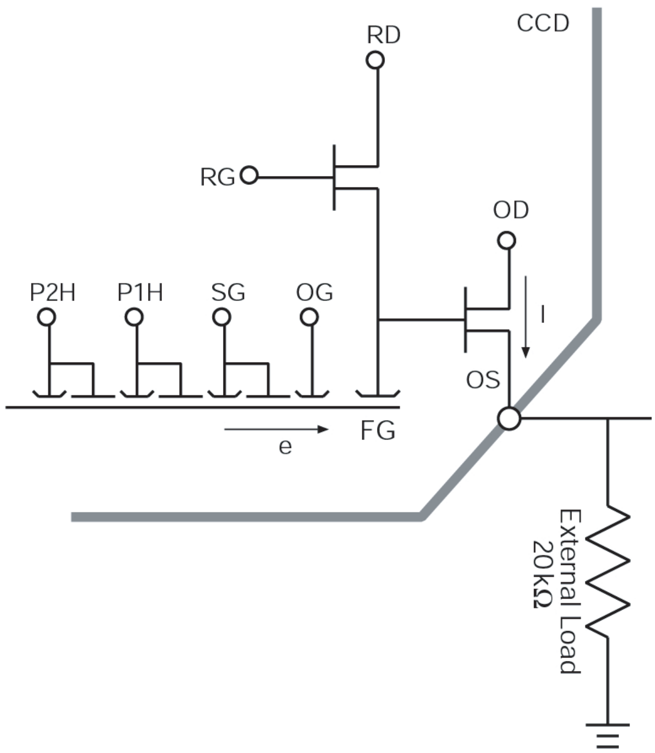


Figure 3.9: Schematic view of the floating diffusion amplifier.

The scheme to measure the amount of charge using the FDA can be explained as follows;

1. SG–Low, RG–High (Reset phase)

   When the reset gate (RG) is clocked high, the drain voltage of MOSFET1 (reset drain: RD) is equal to the source voltage (floating gate: FG). Then the charge stored in the FG is transferred to the RD and is reset.

2. SG–High, RG–Low (Floating phase)

   When RG is clocked low, FG is isolated to RD. The voltage of the FG at this phase is called the “floating level”.

3. SG–Low, RG–Low (Signal phase)

   When the summing gate (SG) is clocked low, the charge stored in the SG is transferred to the FG. The voltage of the FG is then decreased, and is called the "signal level" at this phase. The measurement of the amount of charge stored in a pixel is then completed.

   The scheme backs in the reset phase [1], and the charge is measured in the next pixel.

Figure 3.10shows the typical shape of the output signal (OS) produced by the FDA. The amount of charges stored in each pixel reflects the difference in voltage between those of the floating level and the signal level.

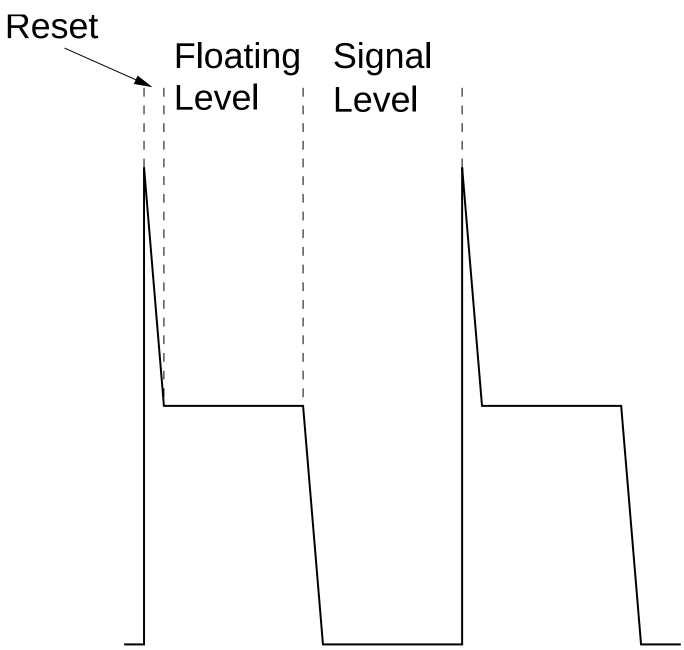


Figure 3.10: Schematic view of the output signal produced by the FDA

The sensitivity of the output amplifier of a CCD is defined by:

$$S_V = \frac{q}{C_s}, \tag{3.12}$$

where S_V is the node sensitivity (V/e$^-$), q is the elementary charge (1.6×10^{-19}C), and C_s is the sense capacitance (F) given by:

$$C_s = C_{MOS} + C_{FD}, \tag{3.13}$$

where C_{MOS} is the gate capacitance associated with the output MOSFET and C_{FD} is the capacitance related to the floating diffusion. These capacitances are essentially determined by the layout design of the FDA. The node sensitivity is the conversion coefficient from the amount of charges to the voltage. Therefore, a high node sensitivity yields a high tolerance for noise from the external system other than the CCD itself.

3.3.2 Mechanism of Charge Measurement

As described in the previous subsection, the stored charge in each pixel is reflected in the gap between the voltage of the signal phase and the floating phase. Next, we briefly explain the major methods to measure the voltage gap.

1. **Delay method**

   Figure 3.11 shows the scheme of the delay method. We divide the OS signal into two, and delay one signal with a delay circuit so that the signal level of the delayed OS signal overlaps with the floating level of the original one. Then, we can detect the voltage difference using a difference circuit. This method is characterized by the combination of the fundamental electrical circuits.

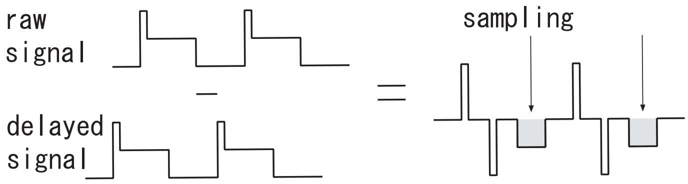
   

   Figure 3.11: Schematic view of the delay method.

2. **Correlated double sampling method (CDS method)**

   The scheme of the correlated double sampling method is shown in Figure 3.12. We sampled the voltage of the floating and the signal phase by ADC in advance, and subtracted each level. By multiple sampling of each phase and averaging, we can decrease the effects of random noise. However, a high-speed ADC is necessary to increase the number of samplings.

3. **Double slope method**

   We show the scheme of the dual slope method in Figure 3.12. Using the integrator circuit, we integrated the floating voltage level onto the integrating capacitor during the timing 1 is high. After integrating the floating level, the signal voltage level is "invertedly" integrated onto the capacitor during the timing 2 is high. After that, the integrated signal shows the voltage level which corresponds to the gap of the voltage level between the signal and floating phase.

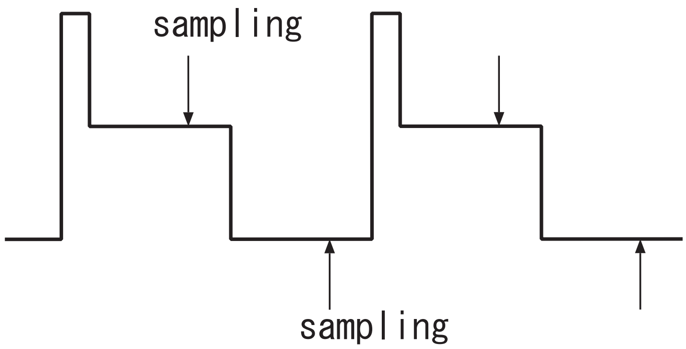


Figure 3.12: Schematic view of the correlated double sampling method.

This method is very effective for removing random noise and does not require a fast ADC. However, the integration filter usually requires a very complicated circuit system, and there is a possibility that we are affected by the noise of the filter itself.

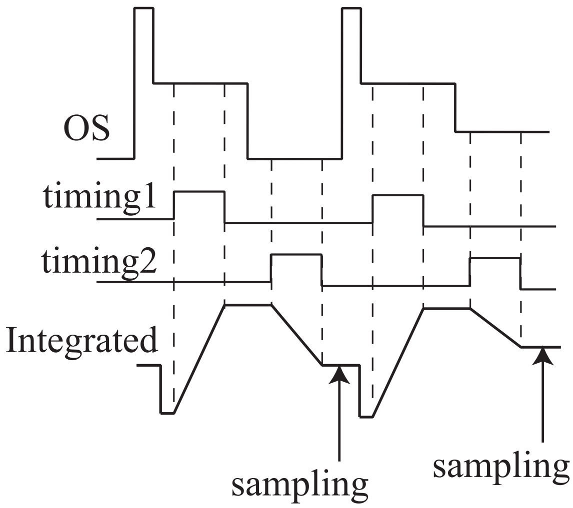


Figure 3.13: Schematic view of the dual slope method.

3.4 Noise Sources

In this section, we describe the factor of noise sources which degenerate the spectroscopic ability of a CCD.

3.4.1 Readout Noise

The readout noise is mainly generated in the MOS transistor which composes the FDA (see Figure 3.9). The noise of the MOS transistor consists of a random thermal noise, $1/f$ (flickering) noise, and kTC (reset) noise.

Thermal noise is generated by the thermal agitation of electrons in channel resistance in the MOS transistor. Therefore, this noise is observed at random and its power spectrum density is constant independent of frequency. The square mean voltage of this noise (V_n^2) converted to its gate voltage is approximated by the following equation:

$$V_n^2 = \frac{8}{3}\frac{kT}{g_m \Delta f}, \tag{3.14}$$

where k is the Boltzmann constant, T is the temperature, f is the frequency, and g_m is mutual conductance.

The $1/f$ (flickering) noise is caused by the capture and emission of electrons at the interface trap level in a channel of the MOSFET. The square mean voltage of this noise (V_n^2) converted to its gate voltage is approximated by this equation [29],

$$V_n^2 = \frac{q^2 d_{ox}^2 n_{Te}}{\epsilon_{ox}^2 W L f}, \tag{3.15}$$

where n_{Te} is the trap concentration in a channel, ϵ_{ox} is the permittivity of a gate oxide, $WandF$ are the width and length of a gate respectively, and q is the elementary electric charge. This equation contains a frequency f in the denominator, therefore, the power spectrum density is proportional to $1/f$. W and F are also present in the denominator, meaning that the $1/f$ noise is governed by that caused in the smallest MOSFET.

Since the $1/f$ noise increases as the frequency is lower, the CDS circuit significantly attenuates the $1/f$ noise, because the frequency response of the CDS falls off with decreasing frequency [72]. Reducing the $1/f$ noise through signal processing via the CDS allows us to reduce the size of the on-chip amplifier. This in turn increases the node sensitivity (V/e$^-$) because we can reduce the gate capacitance associated with the MOSFET amplifier.

Reset noise is generated by the periodic resetting of the readout node by the MOSFET. Since the reset noise is generated every time we reset the readout node, the floating voltage level is different from pixel to pixel. The noise induced on the readout node is caused by the channel resistance of the MOSFET used to reset the FG. The voltage of this noise is shown as:

$$V_n = \sqrt{\frac{kT}{C}}, \tag{3.16}$$

where k, T, and C are the Boltzmann constant, temperature, and capacitance of the FG.

This equation can also be expressed in units of electrons as,

$$N_n = \sqrt{\frac{kTC}{q}}, \tag{3.17}$$

where q is the elementary charge (1.6×10^{-19} C). The reset noise expressed this way is called the kTC noise.

However, the reset noise voltage will not significantly change over a pixel period after the reset switch is turned off (in other words, after RG is low). Therefore, by differencing a sample of floating level and signal level, we cancel out the reset noise because the noise amplitude does not change over the sampling period. In other words, we can completely remove the reset noise by using the delayed method, correlated double sampling, and dual slope methods as described in the previous section.

Dark Current

Dark current is intrinsic to semiconductors and occurs naturally through the thermal generation of minor carriers. If there are imperfections or impurities within the semiconductor or the Si-SiO_2 interface, the energy level occurs in the forbidden bandgap. Then, some electrons are excited to the conduction band from the valence band via the generated energy levels in the forbidden bandgap, mainly by the thermal motion, thereby promoting the dark current. We call this source "dark current" because it is produced even when the CCD is in complete darkness.

There are three principle factors for the generation of the dark current;

1. thermal excitation and diffusion of charges in the field-free layer below the potential well,
2. thermal excitation of charges in the depletion layer,
3. thermal excitation of charges at the Si-SiO_2 interface.

The contribution from surface states is the dominant source of the dark current. However we can reduce this current with the MPP mode [24]. Since dark current is mainly caused by thermal excitation, we can significantly reduce it by cooling the CCD. The relationship between the dark current I_{dark} and the operating temperature T is given by the following equation [35]:

$$I_{dark} \propto T^{1.5} \exp(-\frac{E_g}{2kT}), \tag{3.18}$$

where E_g is the bandgap energy of silicon and k is the Boltzmann constant.

Note that the bandgap energy of silicon E_g varies with operating temperature following the empirical formula [52],

$$E_g = 1.1557 - \frac{7.021 \times 10^{-4} T^2}{1108 + T} [\mathrm{eV}]. \tag{3.19}$$

3.4.2 Charge Transfer Inefficiency

Charge transfer efficiency (CTE) is a measure of how effectively the CCD transfers charge from one pixel to the next. The CTE is defined as the ratio of charge transferred from the target pixel to the initial charge stored in the target pixel. In X-ray astronomy, CTE is specified in terms of charge transfer inefficiency (CTI). CTI , on the other hand, is the fraction of charge left behind in a single pixel transfer and is simply defined as $CTI = 1 - CTE$.

CTI is mainly limited by traps located in the signal channel. The traps in a pixel capture a fixed quantity of charge when the charges are transferred to the pixel. Though the trapped charges are slowly released, they are added to the trailing pixels. The time to release the trapped charge is relatively short, the events which trailing in the direction of transfer are observed. On the other hand, when the time is longer, it becomes difficult to see such a tail. Therefore charges seem to be lost gradually with increasing number of transfers.

Traps can be created during the design and manufacture of the chips, and to some degree, they are also found in the starting silicon material (bulk), even before a CCD is made.

3.4.3 Spurious Charge

Spurious charge is generated when a CCD is clocked into inversion[25]. When the gate voltage is clocked low (a negative voltage), a CCD is in an inverted phase and some holes become trapped at the Si-SiO_2 interface. When the gate voltage is clocked high (a positive voltage), the CCD is switched to a non-inverted phase and trapped holes are accelerated from the Si-SiO_2 interface with sufficient energy to create electron-hole pairs by colliding with silicon atoms. These "spurious " electrons are then collected in the nearest pixel and contaminate the original signal charge.

To reduce the Spurious charge, we reduce the change in the electric field which gives the trapped hole large kinetic energy. We usually avoid the spurious charge by (1) reducing the voltage gap between the high phase and low phase, and (2) slowing down the rise time from the low to the high phase.

3.5 X-ray Detection

In the X-ray band (<50 keV), the interaction between X-ray photons and silicon is dominated by the photoelectric effect, as shown in Figure 3.14.

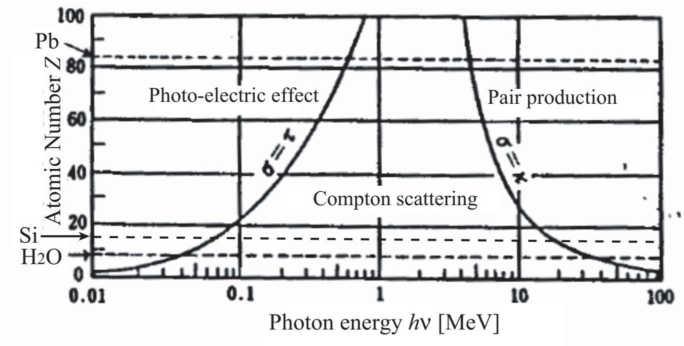


Figure 3.14: Relative importance of the three major types of X-ray and γ-ray interactions. The line shows the value of Z and $h\nu$ for which two neighboring effects are just equal [11].

When an X-ray photon is injected onto a CCD, it is absorbed by a Si atom via the photoelectric effect; the X-ray photon undergoes interaction with a Si atom wherein the photon completely disappears. Then, an energetic photoelectron (a primary electron) is ejected by the atom from one of its bound shells. The kinetic energy of the primary electron is given by,

$$E_{e-} = E_x - E_b \tag{3.20}$$

, where E_x is the energy of the absorbed X-ray and E_b is the binding energy for K-shell electrons (1.74 keV for Si).

The primary electron produces an ionizing trail of electron and hole pairs (e-h) through inelastic collisions with orbital electrons of other Si atoms. The primary electron produces one electron and hole pair per energy of E_{e-h}, which for silicon is 3.65 eV at room temperature [9]. The binding energy used to fill the K-shell again is either converted into another X-ray, or creates additional electron/hole pairs through a mechanism referred to as the Auger process. In the latter case, the atom returns to the ground state when electrons from the outer shells drop to inner ones as free electrons are ejected from the atom. The energy therefore appears largely as kinematic energy of the ejected Auger electrons rather than energy in the form of an X-ray photon. The Auger process occurs with much higher probability than the X-ray emission process. The energy of the absorbed X-ray photon (E_x) is completely transferred to a number of electron and hole pairs. The generated charge is $\frac{E_x}{E_{e-h}}$. If a Si X-ray is produced, it will likely "escape" from the original point of interaction. The net signal generated under these circumstances is only $\frac{E_x - E_b}{E_{e-h}}$, creating an escape peak. The Si X-ray that is produced may be absorbed by the CCD at some other pixel location resulting in an X-ray (Si-K line) charge packet of $\frac{E_b}{E_{e-h}}$ or it may escape from the sensor entirely.

The energy of the incident X-ray photons is estimated by measuring the number of generated electron and hole pairs. As described above, one electron and hole pair is generated per 3.65 eV. Therefore, $\sim 10^3$ electron and hole pairs are generated for an X-ray photon of a few keV.

If all the energy of an X-ray photon was used to produce electron-hole pairs directly, there would be no statistical variation in their amount of charge generated by the X-ray. However, a finite amount of energy is transferred to the Si lattice by non-electron-hole processes (e.g., thermal), giving rise to a small statistical difference in the number of electron-hole pairs actually generated. This uncertainty is characterized by the Fano factor, originally formulated by U. Fano in 1947 to describe the uncertainty of the number of ion pairs produced in a volume of gas following the absorption of ionizing radiation.

Then, the statistical variation of the number of electron-hole pairs are corrected with the Fano factor F as follows,

$$\sigma_x = \sqrt{F \times \frac{E_x}{E_{e-h}}}, \tag{3.21}$$

where E_x is the photon energy. Experimentally, the Fano factor has been determined to be 0.12 for silicon.

In general, the energy resolution is determined by the root mean square of the statistical variation of electron-hole pairs (σ_x) derived in Eq. 3.21 and the system noise in electrons (σ_{noise}) as follows,

$$\Delta\ E(FWHM) = \sqrt{8 \log 2} \times E_{e-h} \times \sqrt{F \times \frac{E_x}{E_{e-h}} + {\sigma_{\mathrm{noise}}}^2}\ [\mathrm{eV}]. \tag{3.22}$$

Examination of Eq. 3.22 reveals that the system noise must be minimized in order to exploit the potential for X-ray spectroscopy offered by the silicon properties. Reducing system noise to $\sim$0 electron results in Fano noise-limited performance down to the energy resolution (FWHM) of 120 eV for an X-ray of 5.9 keV.

3.6 Data analysis

The output signal (OS) of a CCD includes information not only of the signal charge generated by the incident X-rays but also of the offset level caused by the dark current and Spurious charge, as well as variations caused by the readout noise, CTI, and shot noise of the offset. Since the OS is converted to digital data by an ADC, we need to (1) properly subtract the offset level from the digital data to estimate the energy of incident X-rays, and (2) evaluate the noise level to confirm whether we are driving the CCD properly.

In this section, we describe the methods for (1) extraction of X-ray events, and (2) estimation of the performance of a CCD.

3.6.1 Output image of CCD

Figure 3.15 shows the pattern diagram of a typical output image of a CCD. The pixels in the "active region" are really exposed during the exposure time and they contain the digital value corresponding to the charge stored in the exposure and transfer time. In later, we refer to the digital value in each pixel as the "raw pulse height (RPH)". On the other hand, when we repeat the transfer over a number of CCD pixels, the vertical overclocked region (VOC) and the horizontal overclocked region (HOC) are available. These overclocked regions are useful to evaluate the performance of a CCD. The RPH of pixels in the HOC corresponds to the charge which is generated only in the horizontal transfer. The RPH of pixels in the VOC corresponds to the charge which is generated only in the horizontal and vertical transfer. We describe the evaluation of a CCD in detail in the following subsection 3.6.3.

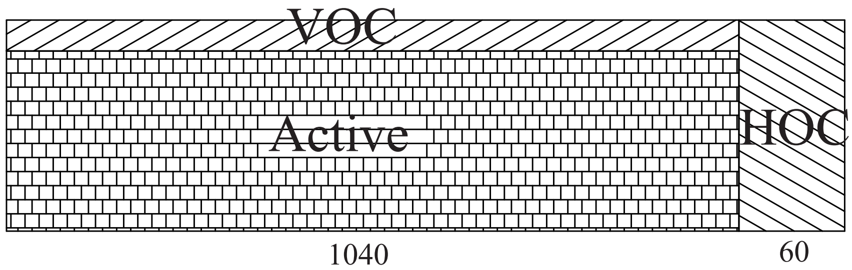


Figure 3.15: Pattern diagram of the typical output image of a CCD. We repeat the charge transfer 1200×300 times for a CCD of 1040×256 pixels.

3.6.2 X-ray event analysis method

The RPH in each pixel has some offset level, even if no X-ray photon enters, which is caused by the dark current, spurious charges and the electrical offset by the FDA. First, we subtract the offset level from the RPH in each pixel. The offset level in each pixel is determined by averaging the RPH using multiple images obtained under the same condition. By subtracting the offset level from the RPH, we obtain the "pulse height" (PH) in each pixel. The PH represents the amount of charges attributed to be X-ray events.

Secondly, we recognize X-ray events from the images containing the PH in each pixel and estimate the incident X-ray energy. As described above, an X-ray photon absorbed in a CCD generates a number of electrons. While these electrons are pulled up to the CCD surface by the electric field in the depletion layer, they are spread by thermal diffusion, and in some case they are distributed over multiple pixels. Since the number of charges is proportional to the incident X-ray energy and corresponds to PH, we have to sum up all the PH spread over multiple pixels. We use two methods to carry out this reconstruction, one is the "grade method" and the other is the "fitting method". In the following, we describe the basic concepts of these methods.

3.6.2.1 Grade Method

The grade method is the standard X-ray events analysis method applied to CCD detectors used in the *ASCA*, *Chandra*, *XMM*, and *Suzaku* satellites. In this method , we sum up all the charges spread over multiple pixels and distinguish X-ray events from others using the following scheme;

1. We pick up pixels which have PH beyond the "Event threshold" and we call these "event pixels"
2. For the charge distribution of 3 × 3 pixels surrounding the event pixel, we pick up pixels which have the PH beyond the "Split threshold". We call these "split pixels". Hereafter, we ignore the pixels which are judged to be neither event pixels nor split pixels.
3. Based on the position pattern of the event pixels and the split threshold, we classify each X-ray event into eight grades (Figure 3.16).
4. We sum up the PH of the event pixels and split pixels. We note that we do not add the PH of some split pixels in some grades.

3.6.2.2 Fitting Method

The fitting method is employed as an alternate solution. For example, this method is usually employed to rectify some X-ray events which are too widely spread to reconstruct using the grade method. We fit the elliptical distribution of the PH on the CCD surface with a two-dimensional non-spherical Gaussian function (see Figure 3.17) [43].

$$Z(X,Y) = \frac{Norm.}{\sqrt{2\pi\sigma_x\sigma_y}} \exp - \frac{(X-x)\cos\theta + (Y-y)\sin\theta^2}{2\sigma_x^2} \frac{(X-x)\sin\theta + (Y-y)\cos\theta^2}{2\sigma_y^2} \tag{3.23}$$

, where

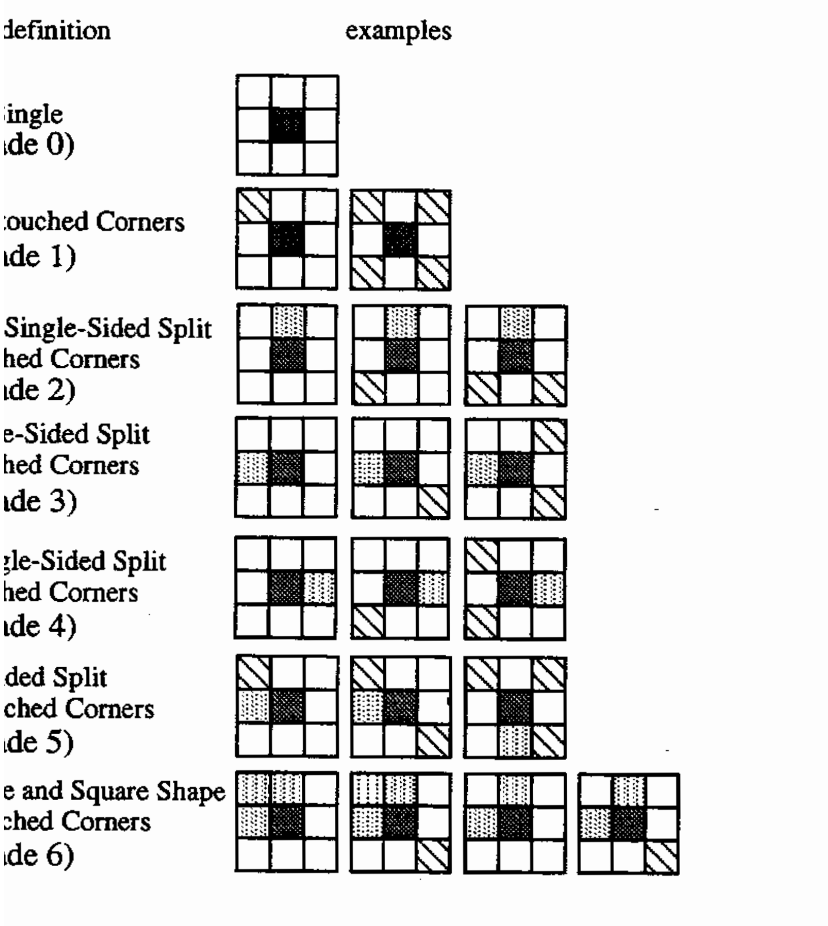


Figure 3.16: criteria of grading pixels into 8 grades. The events that meet none of the criteria (in other words, the more spread ones) are labeled grade 7.

1. $Norm.$: the incident X-ray energy as the total volume of the best fit function corresponds to it.

2. x, y : the position of the incident X-ray events.

3. σ_x, σ_y: ellipticities of the PH distribution.

4. θ : rotation angle between the horizontal axis of the CCD chip and the longer axis of the ellipse.

The total pulse heights (Z) of each 5×5 pixels around the center pixel are calculated based on the position of each pixel (X, Y) using Eq. 3.23, and are fit to the real data. The fitting method has several advantages over the grade method.

(1) This method can be applied to CCDs of any pixel size.

(2) By using this method, we can make use of more spread events, often caused when X-ray photons of higher energy are injected and absorbed in the field-free region, by compensating for the lost charges. These spread events are labeled as grade 7 and discarded when the grading method is used. Thus, we can get higher detection efficiencies, especially in the higher energy band, without significantly degrading the energy resolution.

(3) We can analyze polarized X-ray events using this method. Tsujimoto et al. (2000) [64] showed that the fitting method can determine the degree of polarization and the rotation angle of the polarized X-rays detected by the X-ray CCD.

(4) We do not need a split threshold anymore.

Kohno et al. (2000) [30] successfully measured the relationship between the extent of an event and the X-ray absorption depth. Using this, they showed that the thickness of the CCD depletion layer can be measured without calibrating the absolute flux of the monochromatic X-rays.

3.6.3 Estimation of Noise Level

In this subsection, we describe the method to determine the noise level of the readout noise, the dark current, the CTI and the spurious charge. As described in section 3.6.2, the PH distribution gives us different information in each region of Active, VOC, and HOC.

We summarize the noise sources affecting the PH in each region as follows;

- Active region $\cdots$ readout noise + spurious charge + $\mathrm{CTI_v}$ +$\mathrm{CTI_h}$ + dark current

- VOC region $\cdots$ readout noise + spurious charge + $\mathrm{CTI_v}$ +$\mathrm{CTI_h}$

- HOC region $\cdots$ readout noise

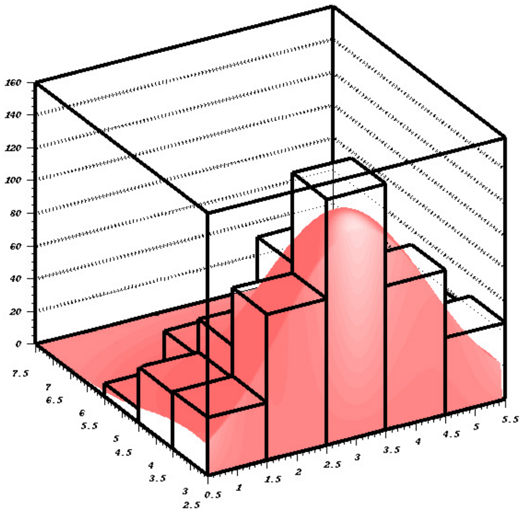


Figure 3.17: Schematic view of the fitting method. The charge distribution of 5×5 pixels are fit with a two-dimensional Gaussian function.

In the following, we describe the method used to estimate the noise level in a concrete form. Except as noted, our derived noise levels of test devices (see chapter 6) are calculated in the following way.

Readout noise The readout noise is derived from the PH distribution in the HOC region since PH in the HOC region suffers less from noise sources other than the readout noise. We define the readout noise as the standard deviation (converted to the number of electrons) of the PH distribution in HOC;

$$\begin{aligned}\sigma_{r.o.n}[\mathrm{e}^-] &= (\text{PH standard deviation of in HOC[ADU]}) \\ &\quad \times \frac{\text{gain[eV/ADU]}}{3.65\ \text{eV/e}^-} \qquad \text{[electron]}\end{aligned} \tag{3.24}$$

Dark current The dark current is derived from a comparison of the PH distribution between VOC and the active region. The essential difference between these two regions is whether they are exposed or not. Therefore the gap of the peak channels of the PH distribution reflect the dark current.

$$\begin{aligned}I_{dark} &= \frac{\text{peakchanne(VOC)} - \text{peakchannel(Active)[ch]}}{\text{(Exposure time[sec])}} \\ &\quad \times \frac{\text{gain[eV/ADU]}}{3.65\ \text{eV/e}^-} \qquad \text{[electron/sec/pixel]}\end{aligned} \tag{3.25}$$

CTI The CTI is derived from a comparison of the X-ray spectra in different areas in the Active region as shown in Figure 3.18. We divided the active region into 2×2 areas. We obtained the spectra of the X-ray photons in each area and compared the peak channels of the spectra.

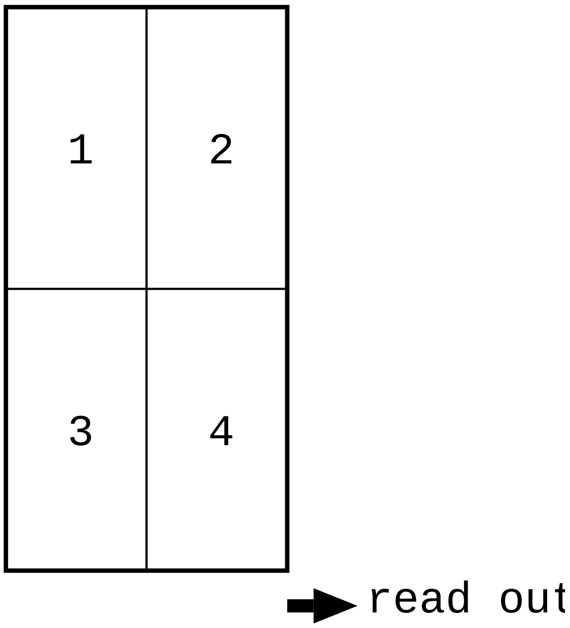


Figure 3.18: Division of the active region to measure CTI.

$$\begin{aligned} \mathrm{CTI}_{\mathrm{vertical}} &= \frac{1}{2}\frac{1}{\text{No. of pix. in vertical}}\left[\frac{(\text{peakchannel}(3)-\text{peakchannel}(1))}{(\text{peakchannel}(3))}\right. \\ &\quad \left. + \frac{(\text{peakchannel}(4)-\text{peakchannel}(2))}{(\text{peakchannel}(4))}\right] \ [\text{pixel}^{-1}] \qquad (3.26) \end{aligned}$$

$$\begin{aligned} \mathrm{CTI}_{\mathrm{horizontal}} &= \frac{1}{2}\frac{1}{\text{No. of pix. in vertical}}\left[\frac{(\text{peakchannel}(2)-\text{peakchannel}(1))}{(\text{peakchannel}(2))}\right. \\ &\quad \left. + \frac{(\text{peakchannel}(4)-\text{peakchannel}(3))}{(\text{peakchannel}(4))}\right] \ [\text{pixel}^{-1}] \qquad (3.27) \end{aligned}$$

Spurious charge The Spurious charge is derived from a comparison of the PH distribution between VOC and HOC. The essential difference between these two areas is whether they are transferred vertically or not. Therefore the gap of the center channels of the PH distribution reflects the Spurious charge mainly generated by the vertical transfer.

$$\begin{aligned} \text{spurious charge} &= [(\text{peakchannel(VOC)}) - (\text{peakchannel(HOC)})] \\ &\times \frac{\text{gain[eV/ADU]}}{3.65\ [\text{eV/e}^-]} \qquad [\text{electron}] \end{aligned} \tag{3.28}$$

Chapter 4

Soft X-ray Imager

4.1 Role of Soft X-ray Imager

As shown in Table 2.1, the SXI covers the energy band of 0.5–20 keV. As described in the previous section, since non-thermal emission begins to dominate in the energy range over 10 keV, the imaging and spectroscopic observations of SXI in the energy band of 10–20 keV is invaluable to explore and investigate the nature of non-thermal emission precisely. Therefore, the detector for SXI is required to have excellent imaging and spectroscopic abilities in this energy regime.

From the view-point of the X-ray CCD being equipped with high spatial and energy resolutions, and moderate time resolution simultaneously, it is difficult to adopt other X-ray detectors with the exception of the X-ray CCD for SXI. An X-ray CCD, as the focal plane detector for X-ray astronomy missions, was first used in the *ASCA* satellite which was launched in 1993. Since then, the X-ray CCD has been established to be one of the standard focal plane detectors and has been adopted by most X-ray observatories, including *Chandra*, *XMM-Newton*, and *Suzaku*. Therefore, the X-ray CCD has yielded actual results as a detector carried on satellites. The major weak point of this CCD however is its relatively low sensitivity to hard X-rays. This is because the CCD has silicon which is a low atomic number (Z) element. To compensate for this weak point, a CdTe detector is added behind the CCD in the WXI. Since the CdTe detector consists of high-Z matter, its sensitivity to hard X-ray photons is much higher compared to a CCD. Figure 4.1 shows a comparison of the sensitivity for a CCD (300-μm thickness) and CdTe (0.5- and 1-mm thickness) . Even a CdTe detector with a thickness of 0.5 mm provides good detection efficiency for the hard X-ray band up to 80 keV.

However, the position resolution of the CdTe pixel detector is $> 200\ \mu$m[12, 59], which is worse than that of an X-ray CCD, and in addition, the energy resolution for the soft X-ray (< 10 keV) band is also worse than that for an X-ray CCD. Therefore, a CCD is still suitable for imaging and as a spectroscopic detector for X-rays below ~ 20 keV.

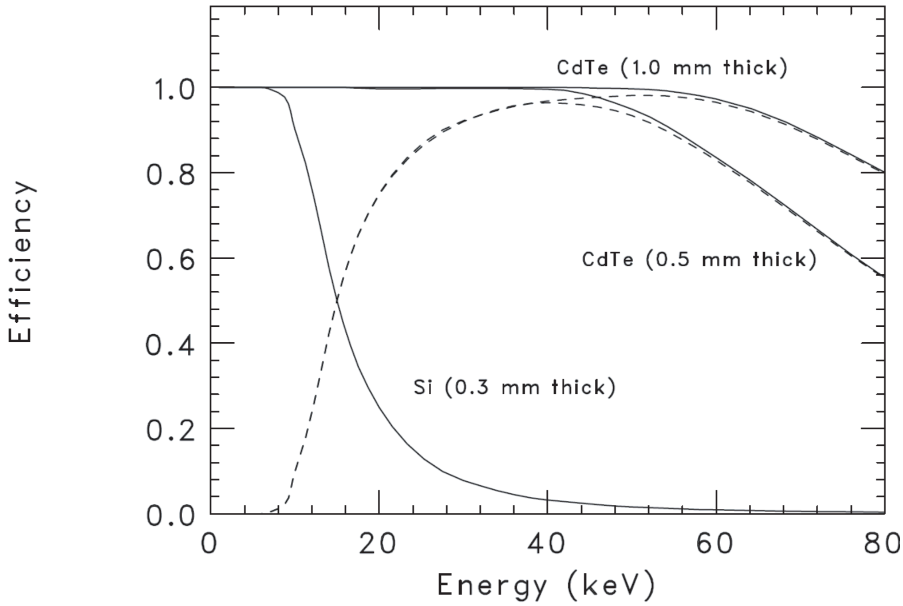


Figure 4.1: Comparison of the sensitivity between a CCD (300-μm thickness) and CdTe (0.5- and 1-mm thickness).

4.2 CCD for Soft X-ray Imager - Back Supportless CCD -

In this section, we first discuss the requirements for a CCD adopted as the SXI. Based on these requirements, we examine the development plan for the SXI.

To detect non-thermal X-ray emission with high sensitivity, we need to improve the detection efficiency in the energy band above 10 keV as much as possible. The detection efficiency of a CCD for X-rays with energies > 10 keV strongly depend on the thickness of its depletion layer (see also section 3.1.1). Figure 4.2 shows the relationship between the thickness of the depletion layer and the detection efficiency of a CCD. It can be clearly seen that the detection efficiency for hard X-rays of 10 keV–20 keV improves significantly with increasing thickness of the depletion layer. Therefore, the thickness of the depletion layer is a key parameter for the development of the SXI.

Another key parameter is the thickness of the field-free region. The CdTe pixel detector (HXI) is present below the SXI to detect hard X-rays which cannot be detected by SXI. However, a standard CCD has a field-free layer other than the depletion layer. Though the depletion layer is sensitive to X-rays, the field-free layer is insensitive to them. Therefore, a fraction of the hard X-rays which cannot be detected by the CCD is absorbed and lost in the field-free region, in other words, this fraction cannot reach the HXI. Since a standard CCD has a thick field-free layer

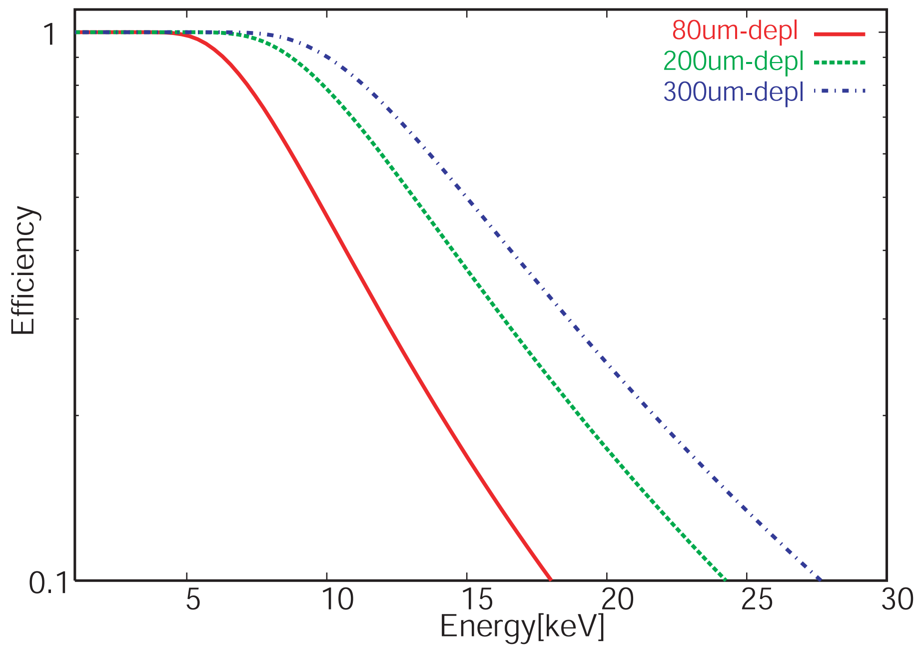


Figure 4.2: Relation between the detection efficiency and the depletion layer thickness of the CCD. The red, green and blue lines shows the detection efficiency in the case of the 80 μm, 200 μm, and 300 μm-thick depletion layers, respectively.

of > 600 μm (*cf.* the thickness of the depletion layer is $<$80 μm), the loss of hard X-rays is not negligible. The field-free region of the CCD for SXI is required to be thinned down as much as possible. Furthermore, the CCD is usually sustained by a package which consists of plastic, ceramic plate, or so on. This package is usually too thick to allow X-ray photons to pass through, and therefore, we need to get rid of this completely as well.

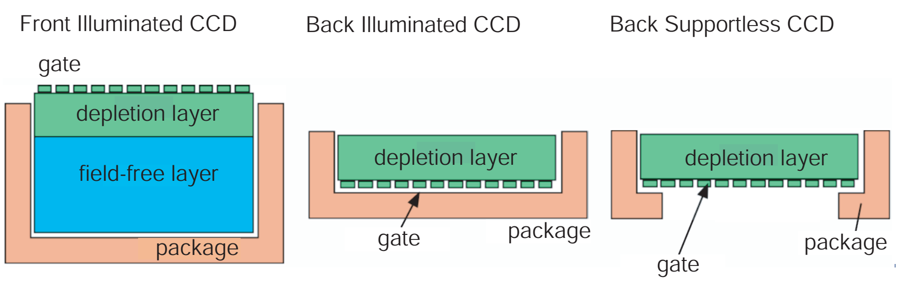


Figure 4.3: Schematic structures of various types of CCDs. (left): normal front illuminated CCD. (center): back illuminated CCD. (right): (back-illuminated) BS-CCD.

Therefore, in order to realize the WXI, two characteristics are primarily required for the SXI which is equipped at the upperstep;

1. to detect soft (< 20 keV) X-rays as much as possible, in other words, to increase the thickness of the depletion layer, and

2. to allow hard (> 20 keV) X-rays to pass through the CCD wafer, in other words, to decrease the thickness of the field-free region and to remove the package.

To satisfy these requirements, we decided to develop a new-type of X-ray CCD **"Back supportless CCD (BS-CCD)"** for the SXI. Our aim was to realize a BS-CCD that has a thick depletion layer and no field-free layer, and package which wastefully absorb X-rays. We anticipated that we needed to develop the BS-CCD gradually, in order to confirm (1) whether such a back supportless structure could be realized, and (2) whether we could produce a BS-CCD with a stable and reliable performance.

In cooperation with Hamamatsu Photonics K.K. (HPK), we have been researching and developing X-ray CCDs for over 10 years. Thus far, we have successfully developed two types of X-ray CCDs at the top international level, the "CCD-CREST"[4] and the "MAXI-CCD"[63, 39]. Table 4.1 shows a comparison of the performance of the CCDs manufactured by HPK with that of the XIS onboard the *Suzaku* satellite, which has the world's highest performance among X-ray CCDs.

Table 4.1: Comparison of *Suzaku* XIS, CCD-CREST, and MAXI-CCD

		Suzaku XIS	CCD-CREST	CCD-CREST2	MAXI-CCD
Readout noise (r.m.s.)	[e-]	2–3	3–5	3–5	<5
Energy resolution[1]	[eV]	130–140	135	135	135
Size of imaging area	[mm^2]	24.5×24.5	24.5×24.5	24×21.6	24.5×24.5
Size of pixel	[μm^2]	24×24	24×24	12×12	24×24
Format[2]	[pix^2]	$1024 \times 1024 \times 2$	$1024 \times 1024 \times 2$	$2000 \times 1800 \times 2$	1024×1024
No. of readout node		4	2	2	1
Depletion layer	[μm]	45(BI), 70(FI)	70	70	80
Illumination type		BI, FI	FI	FI	FI
Transfer method		FT	FT	FT	FFT
Surface coating		(none)	Al	Al	Al

[1] F.W.H.M. of Mn K-α (5.9-keV) line. [2] Sum of imaging area and stored area (except for MAXI-CCD)

We decided to develop the BS-CCD, continuing our cooperation with HPK, for the following reason: It is expected that a number of trial and error steps are needed for the development of the BS-CCD. Therefore, it is rational to select a domestic manufacturer, considering the need for close communication and conferences. In other words, to confirm (1) and (2), HPK was considered to be the best partner manufacturer for developing the BS-CCD. Furthermore, there was no doubt that HPK can produce a CCD with world class performance. In fact, the MAXI-CCD has been carried on the *Hayabusa* satellite [66] and is being driven normally in the space environment. Therefore, it has already been confirmed that the technical capabilities of HPK are sufficiently high in order to manufacture CCDs to be carried on satellites.

Prior to development, it is necessary to decide the goal specifications of the BS-CCD. First, we examine the size of a CCD chip and the back supportless area to allow hard X-rays to pass through.

Since SXI is the best detector in terms of imaging ability on the *NeXT* satellite, we need to enlarge the size of the imaging area of the CCD as much as possible in order to cover as wide a field of view (FOV) as possible. Figure 4.4 shows the vignetting function of HXT [47]. The vignetting function shows the relationship between the effective area and the off-axis angle. In focusing optics, since the reflectivity of the mirror assembly decreases with increasing off-axis angle, the vignetting function shows a hat-like shape, as indicated in Figure 4.4. We note that we normalized the effective area by that at the on-axis in Figure 4.4.

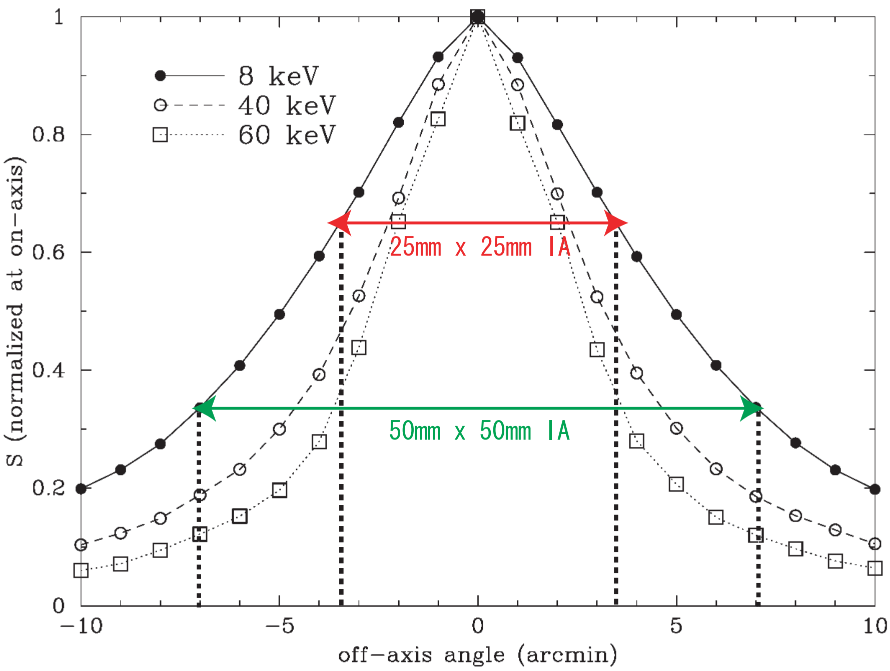


Figure 4.4: The vignetting function of HXT [47].

Based on this vignetting function of HXT, we determined the size of a CCD for SXI. We ensured a wide FOV at least up to the off-axis angle where the normalized effective area at 8 keV is 50 %. Since the focal length between the SXI and HXT is 12 m, 1 arcmin corresponds to 3.4 mm-length at the focal plane. Assuming the IA size is 25×25 mm^2 which is equal in size to that of the XIS, the FOV is $\sim 7 \times 7$ arcmin^2. As seen in Figure 4.4, since the normalized effective area at 8 keV is still maintained high (60 %), we need to enlarge the size of IA in order to make efficient use of HXT performance. The IA size of 50×50 mm^2, which is 2 times wider than that of XIS, corresponds to the FOV of $\sim 15 \times 15$ arcmin^2. This FOV can be achieved (1) by enlarging the IA size of one CCD chip, or (2) by arranging 2×2 CCDs of 25×25 mm^2 size in a mosaic-shaped pattern. Then, the normalized effective area at 8 keV is decreased to $\sim$30 %, therefore we concluded that the IA size of 50×50 mm^2 is a suitable size for the HXT.

The width of the vignetting function is narrower as the X-ray energy is higher, therefore, hard X-ray photons rarely come on the rim of an SXI. Furthermore, the size of the HXI is planned to be 20×30 mm^2. Therefore, we decided to remove the package only at the center of the imaging area. From the view point of mechanical strength and handling, this is clearly a safe approach compared to take the back supportless structure at the whole area of imaging area. Based on the size of the CdTe detector, we made a hole with 30 mm-diameter in the package at the center of the IA.

It is hard to obtain a CCD chip with a large size such as 50×50 mm^2. Since the size of most established X-ray CCD is limited to 25×25 mm^2, it is easily expected that we will face the problem of low process yield when we try to produce a CCD chip which has 4 times larger size than established ones. To cover such a large area, we have a method wherein we arrange CCD chips in a mosaic-shaped pattern (a mosaic CCD camera). This is a reliable method adopted for the *Chandra* and *XMM-Newton* satellites. Figure 4.5 shows pictures of the focal plane of the *XMM-Newton* (left) and *Chandra* (right). Though the IA size per CCD chip in both cameras is $\sim 25 \times 25$mm^2, a mosaic of several CCDs can assure a wide FOV which is over 2 times wider than that of a single CCD chip. However, as seen in Figure 4.5, we cannot avoid the gap between each CCD chip.

Our objective is to fabricate a large-sized CCD with an IA of $\sim 50 \times 50$ mm^2. However, in order to reduce the risk of failure in its development, we also planned to fabricate a medium-sized CCD with a $\sim 25 \times 25$ mm^2 IA. If the development of the large-size CCD is not found to be promising, we will adopt a 2×2 mosaic with the medium-sized CCDs. We note that, in the case of the fabrication of the large-size CCD, we need to process four of the same CCDs, electrically separated from each other, on the same wafer. This is because in this way, we diversify the risk that the whole of the CCD could break down at once, by imparting electrical redundancy to the system.

Next, we examine the performance required for the BS-CCD. As described above, the key parameters are the thickness of the depletion layer and the field-free layer. Based on these for developing the CCDs, we established a “Baseline plan” and a ”Goal plan” to develop the BS-CCD. The former is a conservative plan in which the number of new development items is comparatively small. On the other hand, the latter is an innovative plan aimed at progressively high performance for the BS-

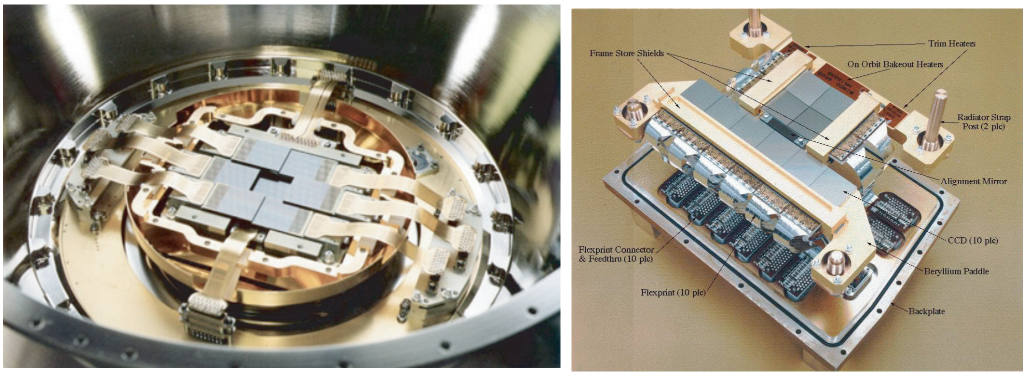


Figure 4.5: Examples of a mosaic CCD camera. (Left) A picture of the focal plane of *XMM-Newton* EPIC-MOS. There are seven FI-CCDs. The size of IA is $\sim 25 \times 25\mathrm{mm}^2$, so that a mosaic of seven covers a focal plane 62 mm in diameter. (Right) A picture of the focal plane of the *Chandra* ACIS. A central mosaic of four FI-CCDs is the imaging array. The size of IA is $\sim 25 \times 25\mathrm{mm}^2$, so that a mosaic of seven covers the focal plane of $\sim 50 \times 50$ mm^2-square.

CCD. We show schematic views of the BS-CCDs produced with the baseline and the goal plan in Figure 4.6

In the baseline plan, we develop the BS-CCD based on CCDs already developed by HPK as well as by us. We selected an FI-CCD, since CCDs with a thick depletion layer ($70-80$ μm) were fabricated as FI-CCDs (see Table 4.1). For reasons related to manufacturing, it is difficult to fabricate BI-CCDs with a thick depletion layer using the conventional method. Additional details are included in the following section 6.1.2.

In the goal plan, however, we have the challenge to develop a BI-CCD with a thick depletion layer of 200 μm. To achieve such a device, it is necessary to change the type of wafer from a p-type semiconductor, used conventionally, to an n-type semiconductor. Though this change is drastic and has the risk of failure in development, the n-type semiconductor has the potential to realize an unprecedentedly thick depletion layer. We will describe the details of these plans in the next section.

The goal for the readout noise and energy resolution is < 5 e$^-$ and 135 eV at 5.9 keV, respectively. Judging from the technical achievements of CCDs fabricated by HPK (see Table 4.1), these goals are considered to be achievable.

Furthermore, we aim to coat the surface of a CCD chip with aluminum. Since the CCD is also sensitive to optical photons, the aluminum evaporation plays the role of a filter for optical blocking. This is also useful to simplify the structure of the SXI because we no longer need to assemble additional optical blocking filters. In the case of the *Suzaku* XIS, since it has no surface Al coating layer, it needs an optical blocking filter, making the structure of the XIS to become complicated. As described in chapter 7, aluminum evaporation has the advantage of significantly

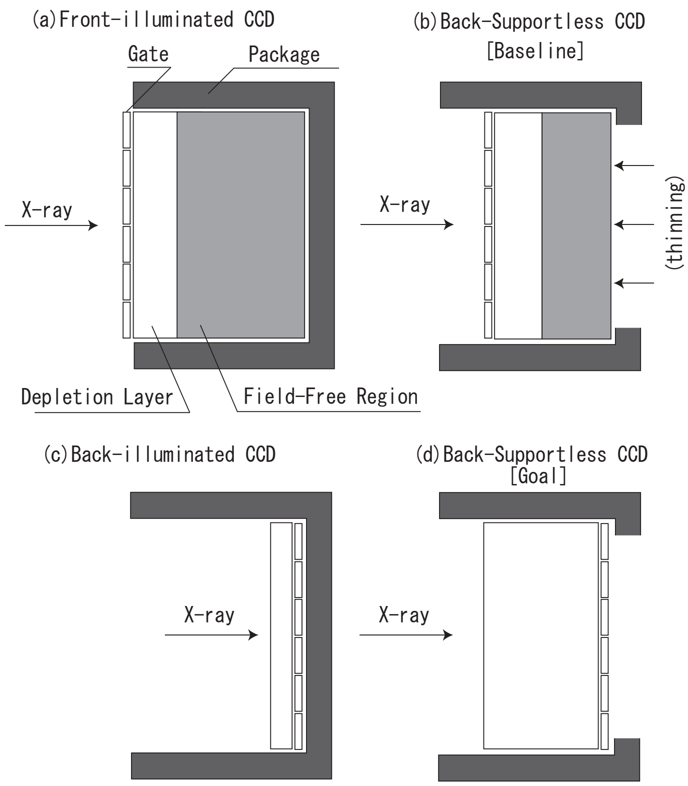


Figure 4.6: The schematic structures of various types of CCDs. (a) Front-illuminated CCD. (b) Front illuminated BS-CCD (the baseline plan). (c) Back illuminated CCD (d): Back-illuminated BS-CCD (the goal plan).

reducing the heat input to a CCD chip by thermal radiation. HPK has already successfully developed a CCD with a surface Al coating (see Table 4.1), therefore this goal is also considered to be very promising.

The goal performance of the SXI is summarized in Table 4.2. For comparison, we also show the performance of the *Suzaku* XIS.

Table 4.2: Comparison of the performance of the baseline and goal plans.

Item	Baseline plan	Goal plan	*Suzaku* XIS
Readout noise	$< 5e^-$		$< 3e^-$
Energy resolution†	135 eV		130 eV
Wafer type	N channel	P channel	N channel
Imaging area	50 mm $\times$ 50 mm		24.5 mm $\times$ 24.5 mm
Back supportless area	30mmϕ		(none)
Pixel size$^\flat$	24 $\times$ 24 μm^2		24 $\times$ 24 μm^2
Depletion layer	70–100 μm	200 μm	70/45 μm (FI/BI)
Field-free layer	50–80 μm	0 μm	$>$ 500/0 μm (FI/BI)
Illumination type	FI	BI	FI/BI
Surface coating	Al	Al	(none)

†: Energy resolution for X-ray of 5.9 keV (FWHM).
‡: Size of Imaging area per a CCD chip.
$^\flat$: Values in active region.

4.2.1 Baseline Plan

Most X-ray CCDs onboard X-ray observatories as focal plane detectors are "N-channel CCDs" (Nch CCDs). Nch CCDs are fabricated on a p-type silicon semiconductor. Since the major carrier in a p-type semiconductor is a hole, the electron is the transferred carrier. The mobility of electrons is higher than that of holes (see Figure 4.7), so p-type semiconductors have an advantage in terms of high speed transfer. Therefore most consumer products and CCDs for scientific use employ Nch CCDs.

Our aim is to achieve the baseline plan based on the established method of fabrication of the Nch CCD as the CCD-CREST and MAXI-CCD in cooperation with HPK. First, in order to confirm the realization of the BS-CCD to investigate any problems in the production process, we process and evaluate a small-sized (12×12 mm^2) test CCD model with the same wafer used in the MAXI-CCD and the CCD-CREST/CREST2. After confirming that there is no performance degradation due to the wafer thinning process, we construct an evaluation model "CCD-NeXT1". This device is a medium-sized (24×24 mm^2) CCD which can be loaded on a satellite. After the development of the CCD-NeXT1, we fabricate a flight

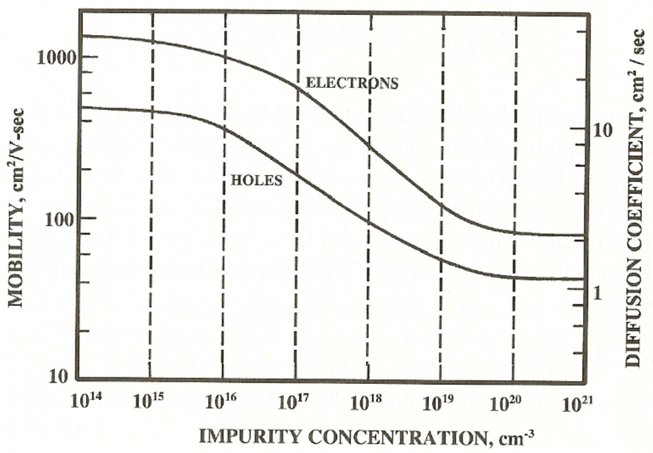


Figure 4.7: Electron and hole mobility as a function of impurity concentration. The electron mobility is about 3 times larger than that of holes independent of the concentration of the impurity.

model "CCD-NeXT2", which will be carried on the satellite. As per the plan, the CCD-NeXT2 is also medium-sized (24×24 mm^2). In order to arrange them next to each other with as little a gap as possible, the CCD-NeXT2 will need to have a buttable structure with a dead region less than 250 μm wide on three sides. Then, the gap between the adjacent two CCDs is restrained to $\sim$ 500 μm. We note that since the CCD-CREST/CREST2 and the MAXI-CCD have a buttable structure, we consider that there should be no problem in the fabrication of a buttable CCD. Figure 4.8 shows the picture of a mosaic camera with 8 CCD-CRESTs. Thanks to a 3-side-buttable structure, this camera achieved a large-size imaging region of 50×100 μm^2.

4.2.2 Goal Plan

The other candidate for the SXI is the P-channel CCD (Pch CCD). This device is fabricated with a MOS-type CCD on an n-type silicon semiconductor. Thanks to the high-resistivity of the n-type silicon, the Pch CCD has the potential to have a thicker depletion layer than the Nch CCD. The Pch CCD was first fabricated by a group at the Lawrence Berkeley National Laboratory (LBNL)[14][18]. They fabricated a back-illuminated and fully depleted CCD on high resistivity ($10\text{k} - 12\text{k}\Omega \cdot \text{cm}$) n-type wafer. They reported the thickness of the depletion layer in their CCD to be $\sim 300\mu$m, which is $\sim$ 4 times thicker than that of established MOS CCDs such as in *Chandra* ACIS, *XMM-Newton* EPIC-MOS and *Suzaku* XIS. Furthermore, the wafer is fully depleted, in other words, no field-free layer exists. Therefore, it is very easy to have the back-illuminated structure. This device acquires high sensitivity for low-energy X-rays (soft X-rays) by the back-illuminated structure

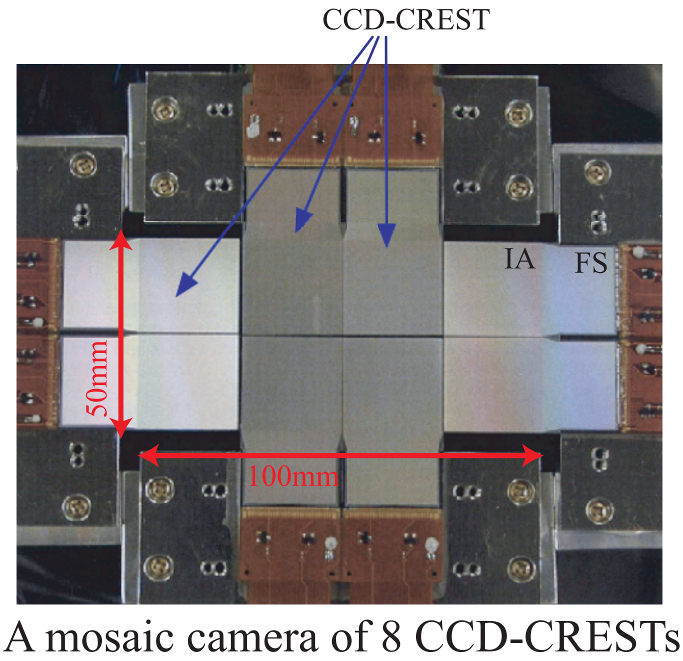


Figure 4.8: A mosaic camera with 8 CCD-CRESTs. Thanks to the 3-side-buttable structure, a large-sized imaging region of 50×100 mm^2 is achieved.

and high sensitivity for high energy X-rays (hard X-rays) by the thick depletion layer, simultaneously.

Judging from the device fabricated by LBNL[14], the Pch CCD is ideal for the BS-CCD, if it can be realized. However, there are no actual results for the Pch CCD as a sensor for astronomy observations. In Japan, a group of the National Astronomical Observatory of Japan (NAOJ) is developing the Pch CCD as a fully-depleted CCD for an infrared and optical sensor [27] in cooperation with HPK. They are developing the Pch CCD for use in the HyperSuprime[31], which is one of the focal plane detectors of the *Subaru* telescope. The Pch CCD is also an attractive image sensor in the optical band because the thick depletion layer depth greatly improves the sensitivity for longer wavelengths ($>$ 700 nm). In fact, Kamata et al. (2004) reported a test device of the Pch CCD which achieved a high quantum efficiency of $> 60\%$ at 1 μm, which is roughly 5$\sim$6 times higher than that of ordinary CCDs [27]. We have adopted the Pch CCD for the goal plan of the SXI and to participate in the development which is proceeded by NAOJ.

First, we evaluate the performance of test models of Pch CCD. In particular, we need to confirm whether (1) the depletion layer is thicker than that in the Nch CCD, and (2) the wafer is fully depleted. After confirming that there are no problems in the small-sized test devices (12×12 mm^2 and 24×6 mm^2) and that the achievement of excellent performance, which meets the demands for the goal plan, is reliable, we

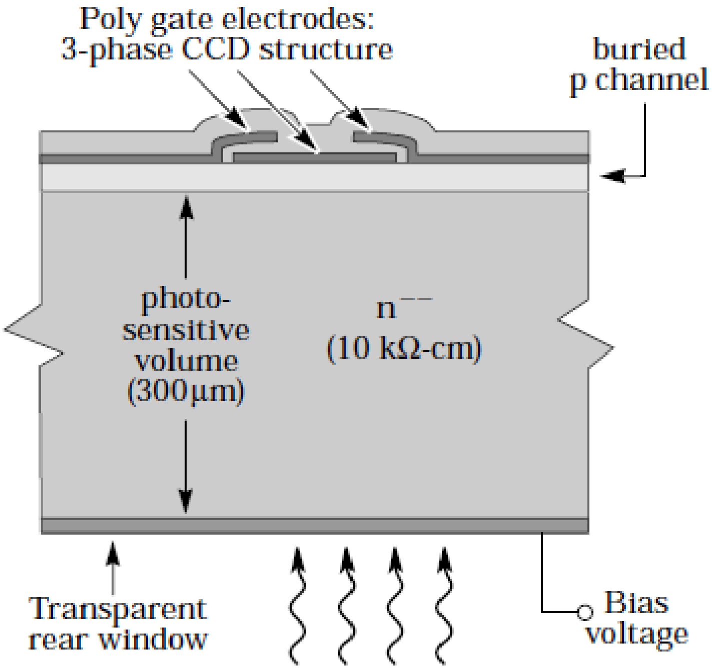


Figure 4.9: Structure of the LBNL Pch CCD[14]. The gate structure, on top of the insulating oxide and protective nitride layers, is conventional, as is the buried channel. A bias voltage on the back window/ electrode depletes the entire substrate.

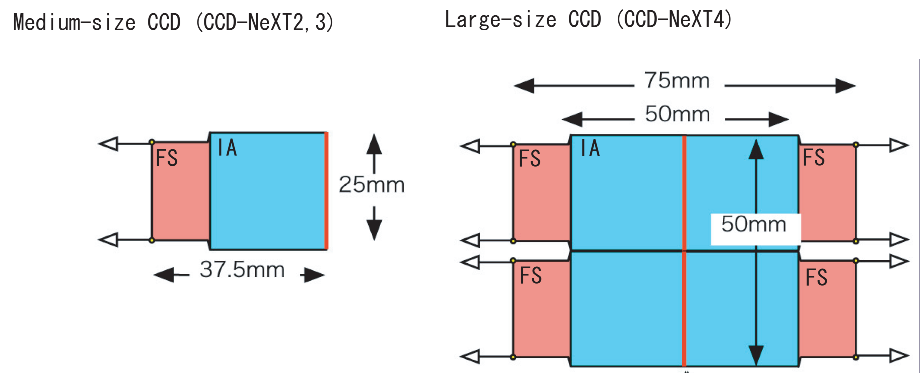


Figure 4.10: Schematic view of the medium-size CCD (left) and large size CCD (right). The large imaging area of 50×50 mm^2 is realized by (1) the mosaic of 2×2 medium-size CCDs or (2) single large-size CCD.

will proceed with the development of the Pch CCD with the following steps; (1) We fabricate a medium-sized (25×25 mm^2) Pch CCD as the "CCD-NeXT3". This device will be fully depleted and the thickness of the depletion layer will be 200 μm. We fabricate this using the process established for the test device, and confirm that there is no problem in performance even if the size of the CCD chip becomes large. (2) After the successful development of the CCD-NeXT3, we will fabricate a large-sized (50×50 mm^2) Pch CCD as the "CCD-NeXT4". As in the case of the CCD-NeXT3, this device will have a fully-depleted wafer of 200 μm-thickness. As described in the above section, we will fabricate four of the same CCDs, which are electrically isolated from each other, on a single wafer. There is the possibility that we will fail in the development of the CCD-NeXT4 because it is an unprecedented large-sized CCD. In this event, we will adopt the CCD-NeXT3 for the SXI. As shown in Figure 4.10, the mosaic of the 2×2 medium-size CCDs covers the required large imaging area of 50×50 mm^2. In Table 4.3, we summarize the comparison of the evaluation and flight models of the baseline and goal plans.

Table 4.3: Comparison of the specifications of the evaluation/flight models of the baseline and goal plans

Code	CCD-NeXT1	CCD-NeXT2	CCD-NeXT3	CCD-NeXT4
Plan	Baseline		Goal	
Purpose	evaluation	flight	evaluation/flight	flight
Readout noise	$< 5e^-$			
Energy resolution†	135 eV			
Imaging area ‡	24×24 mm^2	25×25 mm^2	25×25 mm^2	50×50 mm^2
Format♭	2000×2000	1024×1024	1024×1024	2048×2048
Pixel size♭	12×12 μm^2	24×24 μm^2	24×24 μm^2	24×24 μm^2
No. of nodes	2	2	4	8
Depletion layer	80 μm	70–100 μm	200 μm	200 μm
Field-free layer	70 μm	50–80 μm	0 μm	0 μm
Illumination type	FI	FI	BI	BI
Buttable	N/A	3-side	3-side	N/A
Transfer method	FT	FT	FT	FT
Surface coating	Al	Al	Al	Al

†: Energy resolution for X-ray of 5.9 keV (FWHM).

‡: Size of imaging area per a CCD chip.

♭: Values in active region.

Chapter 5

Experimental Setup

In this chapter, we give an overview of the experimental setup and data acquisition (DAQ) system used for the evaluation of CCDs.

5.1 Data acquisition system

The DAQ system of CCDs consists mainly of a " CCD driver system" and a "read-out system". The CCD driver system generates the clock and bias voltages, and supplies them to the CCD. The read-out circuit (1) amplifies the output signal from the CCDs, (2) shapes its waveform, and (3) changes it to a digital signal. We give brief explanations for these systems in the following paragraph.

CCD driver system As shown in block diagram in Figure 5.1, the CCD driver system consists of two parts; the digital generator (Logic Analyzer TLA 714, Tektronix) and the clock generator. The digital generator gives the high/low phase information of each clock. The time resolution of the TLA 714 is 50 nsec, which is enough fast to activate the CCD clock (usually up to 100 kHz transfer). The clock generator converts the digital clocking pattern provided to the digital generator to analog signals. We use one circuit board of the clock generator to generate one clock. The block diagram of this circuit board is shown in Figure 5.3. The circuit boards are arranged in a special case as shown in Figure 5.2 (lower right). We can freely adjust the voltage levels of the high/low phases of the clocks within the range of -20V to +20V and change the rise and decay time of the clocks by adjusting the variable resistance mounted on the circuit board of the clock generator. Since the digital signal is supplied to the clock generator via a photocoupler, the HCPL-2730 (see Figure 5.3), the analog ground is separated from the digital ground. Clocks generated in the above process are supplied through the CCD head board and drive the CCD.

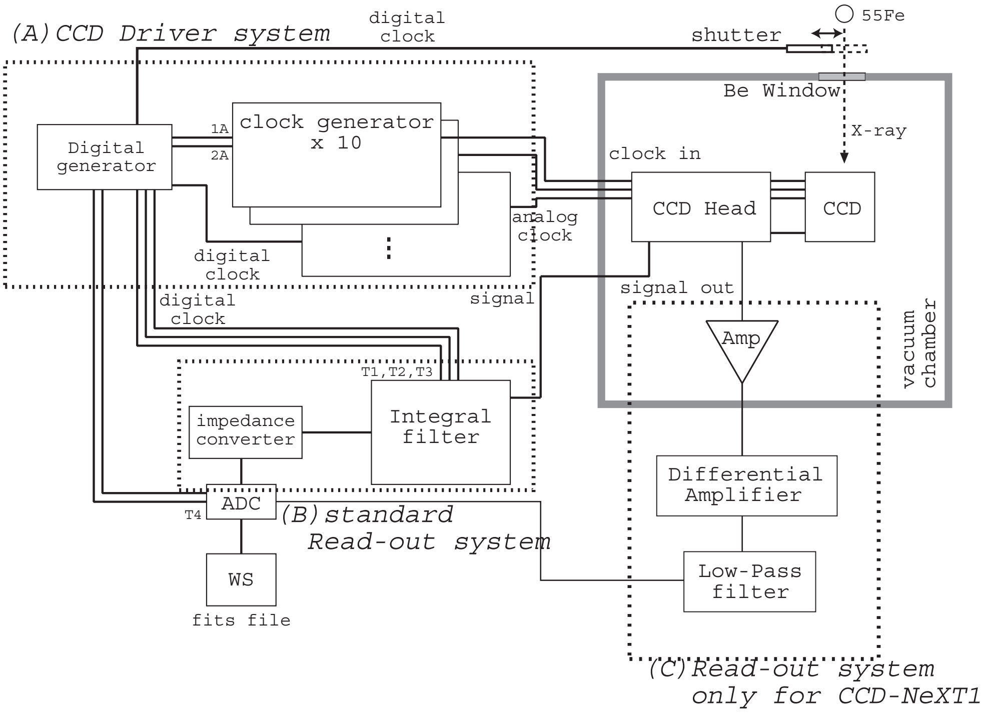


Figure 5.1: Block diagram of the DAQ system. The CCD driver system is shown by the dotted square (A). To process the CCD output signal, we usually use a standard read-out system shown by the dotted square (B). Only in the case of the evaluation of CCD-NeXT1 do we use the read-out system shown by the dotted square (C).

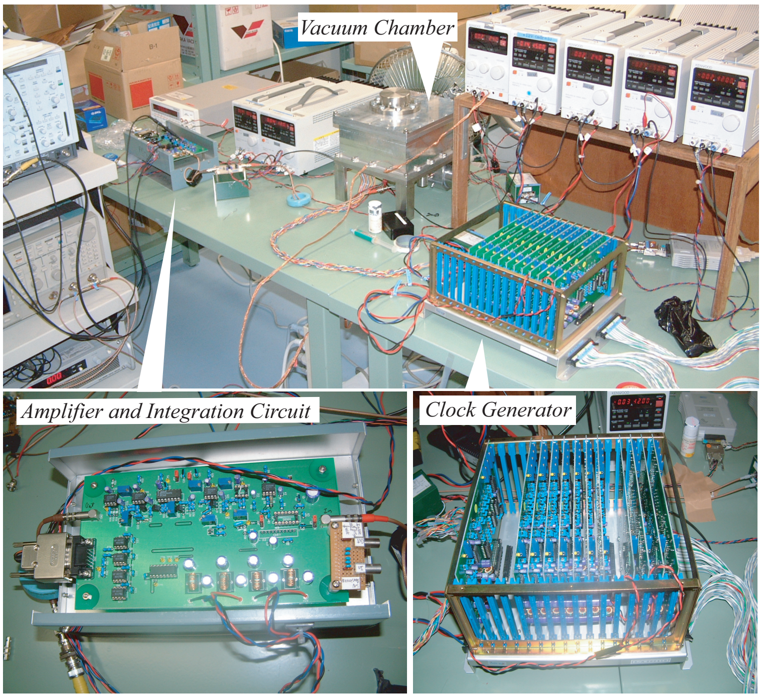


Figure 5.2: Picture of the DAQ system of the CCD evaluation system.

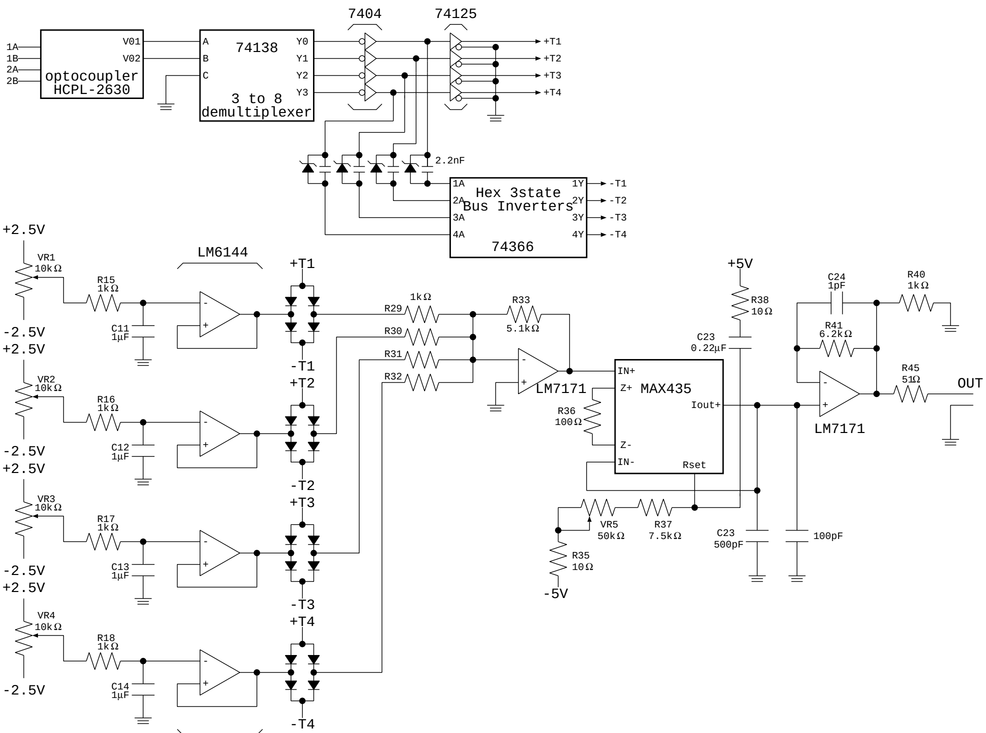


Figure 5.3: Circuit diagram of a board of the clock generator.

Read-out system An output signal is processed with an amplifier and integration circuit, named the "integral filter" in Figure 5.2 (lower left). We show a diagram of the circuit board of the integration filter in Figure 5.4. In this filter, the CCD signal is first amplified by two amplifiers. The output is then fed into an integrating amplifier used a MAX WTA (wide-band transconductance amplifier), the MAX 435[1]. Then, we obtain the integrated charge that is proportional to the voltage gap between the signal and float level in a condenser. In the following circuit, we convert the charge to the voltage and shift within ±10V, which is the input voltage range of the ADC. This processed signal is finally sampled by a 12-bit ADC according to the timing trigger generated by the digital generator.

We note that only in the case of the performance test of CCD-NeXT1 (see chapter 6), we use another read-out circuit consisting of a pre-amplifier, differential amplifier, and low-pass filter (see part (c) in Figure 5.1 and Figure 5.5). The CCD driver circuit is the same as that explained above.

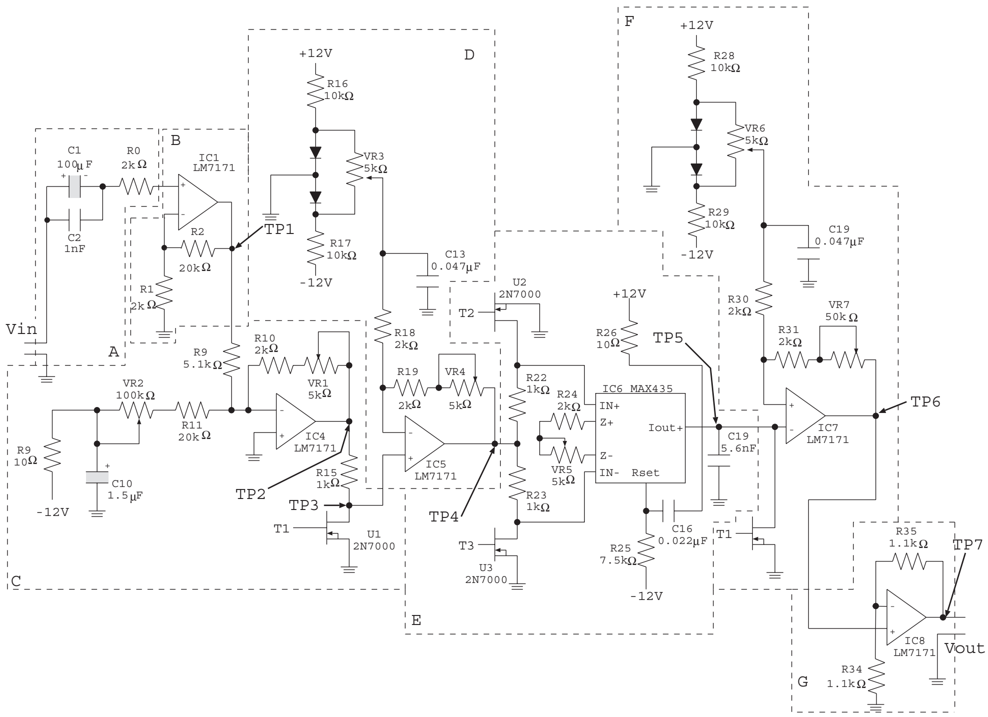


Figure 5.4: Circuit diagram of a board of the integration filter.

[1]Datasheet is available at the following web site; `http://pdfserv.maxim-ic.com/en/ds/MAX435-MAX436.pdf`

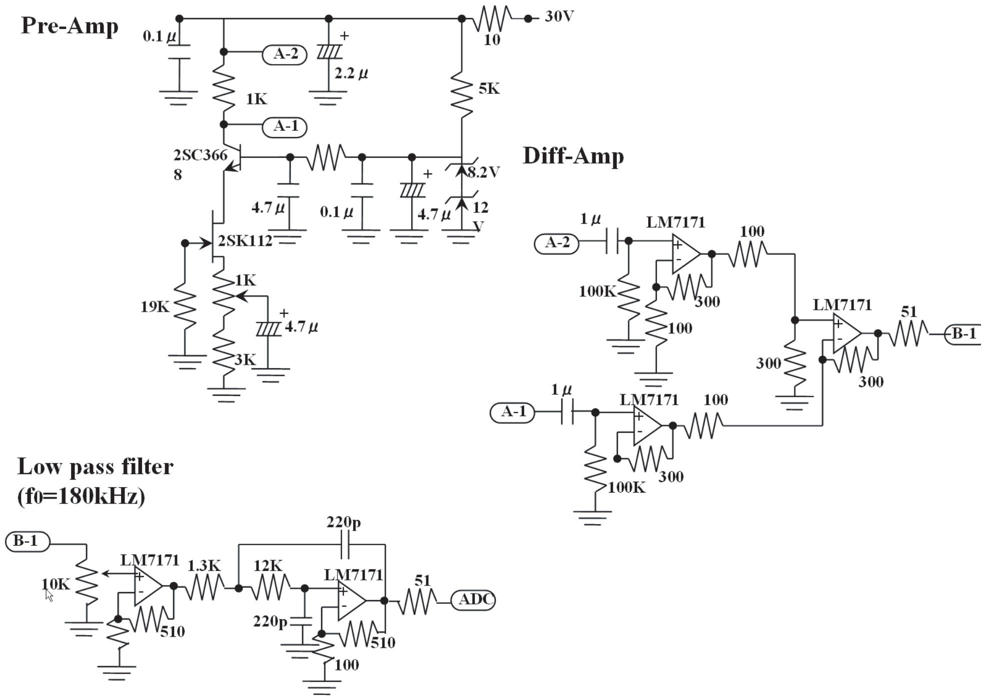


Figure 5.5: Circuit diagram of a readout circuit which is used only for the CCD-NeXT1.

5.2 Overview of the CCD evaluation system

We built two evaluation systems, (1) a multipurpose CCD camera (mini chamber) system and (2) a large chamber system. The former is mainly used for the evaluation of small-size test devices of Nch and Pch CCDs (see chapter 6). The latter is used for the evaluation for the CCD-NeXT1 because the CCD-NeXT1 is too large for the former system (see section 6.1.3).

5.2.1 Multipurpose CCD camera (Mini chamber) system

The X-ray CCD is generally driven in a cool temperature environment to reduce the dark current. We cooled it down in a vacuum chamber to prevent the formation of any water condensation. To make the evaluation of the CCD smooth, we built a "Multipurpose CCD camera (Mini chamber) System" consisting of a mini-size vacuum chamber and a Stirling cooler, SRS-2110 (SHI cryogenics group, Japan). The small size of this chamber allows for its evacuation in a short time. The Stirling cooler has benefits in the following respects; (1) it is easy to install a camera system because of its compact size, and (2) we can easily cool the CCD device without any cooling medium such as liquid nitrogen.

Figure 5.6 shows a photograph (left) and a schematic view (right) of the vacuum

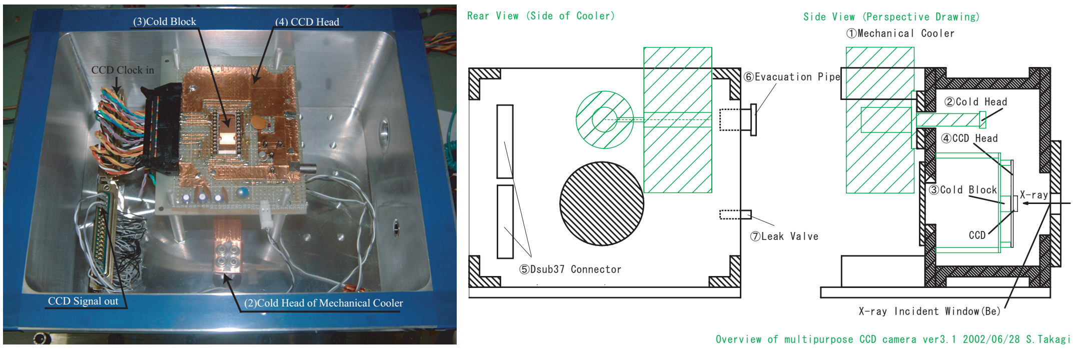


Figure 5.6: (left) Picture of the vacuum chamber. The volume of this chamber is $22 \times 17 \times 8$(depth)cm. (right) Schematic view of the vacuum chamber.

chamber. The Stirling cooler is attached to the under-body of the chamber. Only the cold head is placed in the chamber, so that we need to air-cool the metal cylinder sealed in the Stirling-cycle engine. By using a flexible copper wire braid, we joined the cold head and the cold block contacting the CCD package directly. The CCD clock and the CCD output signal are transferred via the hermetically-sealed D-sub 37 connector attached to the underbody of the chamber. The CCD head circuit can be quickly changed according to the package configuration and pin assignment of the CCD.

Setup for performance evaluation

We irradiate X-rays with the configuration shown in Figure 5.7. X-rays from sealed radio isotopes enter the CCD in the chamber through the thin Be window with < 1 mm-thickness and 3 cm diameter. To block X-rays in the transfer phase, the mechanical shutter is placed in front of the Be window.

Setup for measurement of the depletion layer thickness

We estimate the thickness of the depletion layer ($d_{\rm DL}$) from the detection efficiency($f_{\rm eff}$) using the following formula for the photo-electric absorption:

$$f_{\rm eff} = 1 - exp(-\mu\rho d_{\rm DL}), \tag{5.1}$$

where μ and ρ are the mass-absorption coefficient and the density of silicon, respectively.

To obtain $f_{\rm eff}$, we need to know the absolute flux of the X-rays entering the CCD. The X-rays from the sealed radio isotopes are collimated using the collimator as shown in Figure 5.8.

Since X-rays are collimated into a small size, all the X-rays from the collimator enter the IA of CCD. Figure 5.9 shows the image of the X-rays acquired from the

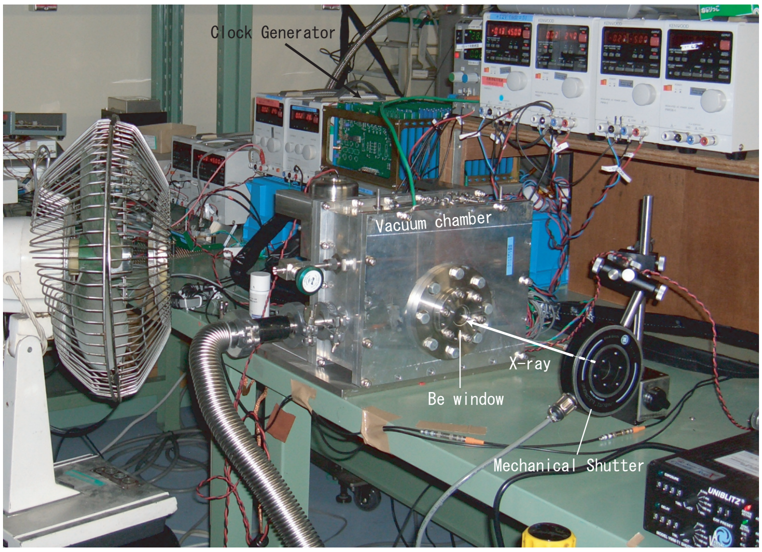


Figure 5.7: Picture of the experimental setup for the performance evaluation test. X-rays from the sealed radio isotope enter the CCD through the mechanical shutter and Be window.

collimator. We can clearly see that the spot size of the X-rays is sufficiently small compared to the size of the imaging area of a CCD. We obtain the flux of the detected X-ray events, divide it by the absolute flux calibrated with the X-ray detector whose detection efficiency is well-known, and then finally obtain the detection efficiency. Since the flux of the collimated X-rays is weak, the exposure time is usually much longer than the transfer time. The number of events detected in the transfer phase is expected to be negligible and can be ignored, compared to that of the exposure phase, therefore we do not use the mechanical shutter in this setup.

5.2.2 Large chamber system

The large chamber system is used only for the purpose of evaluating the CCD-NeXT1. As described in the following section (section 6.1.3.3), the CCD-NeXT1 is a large-size device, and has a flex printed cable and special connectors in anticipation of it being loaded on the satellite. Therefore, the vacuum chamber of the multi-purpose camera system described above is too small to contain it. Thus, we use the large-size ($80 \times 50 \times 50$ cm) chamber. An overview of the system used can be seen in Figure 5.10.

We use the Pulse Tube Cryocooler (Iwatani Industrial Gases Corp.) to cool down the CCD. The stainless (SUS) flexible wire braid joins its cold head and the CCD-NeXT1. The CCD-NeXT1 can be cooled down to ~ -80 °C. Since the transfer method of the CCD-NeXT1 is frame transfer, the mechanical shutter is basically

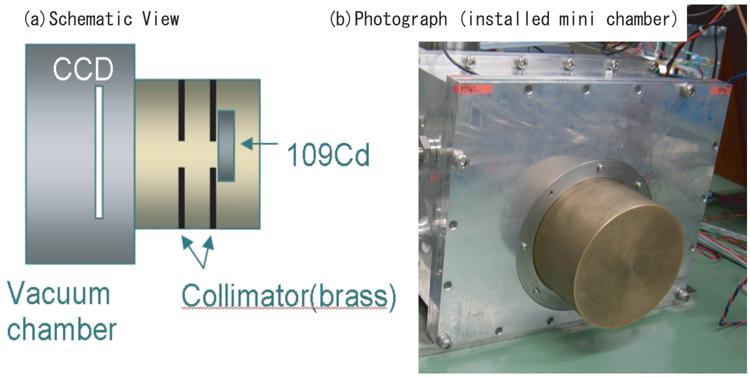


Figure 5.8: Collimator of ^{109}Cd for measurement of the depletion depth. (a) A schematic view of the collimator. X-rays from ^{109}Cd are collimated by two thick brass collimators. (b) Picture of the collimator installed on the mini chamber system.

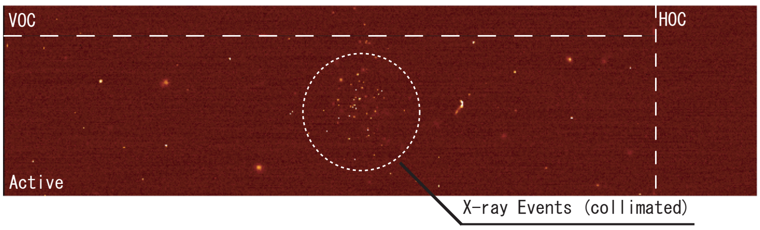


Figure 5.9: The acquired image of the collimated X-rays of ^{109}Cd. The spot size of the collimated X-rays (dotted circle) is small enough comparing the size of active area.

unnecessary. The frame stored area is covered by a thick Al plate so that X-rays cannot enter the CCD in the transfer phase.

As described in the previous section, the readout system is different from the multipurpose CCD camera system. The output signal is first amplified by the preamplifier in the vacuum chamber, second by the differential amplifier, and finally filtered by the low-pass filter (see Figure 5.5). The differential amplifier and the low-pass amplifier are located outside the vacuum chamber. The CCD driver circuit is the same as that of the multipurpose CCD camera system.

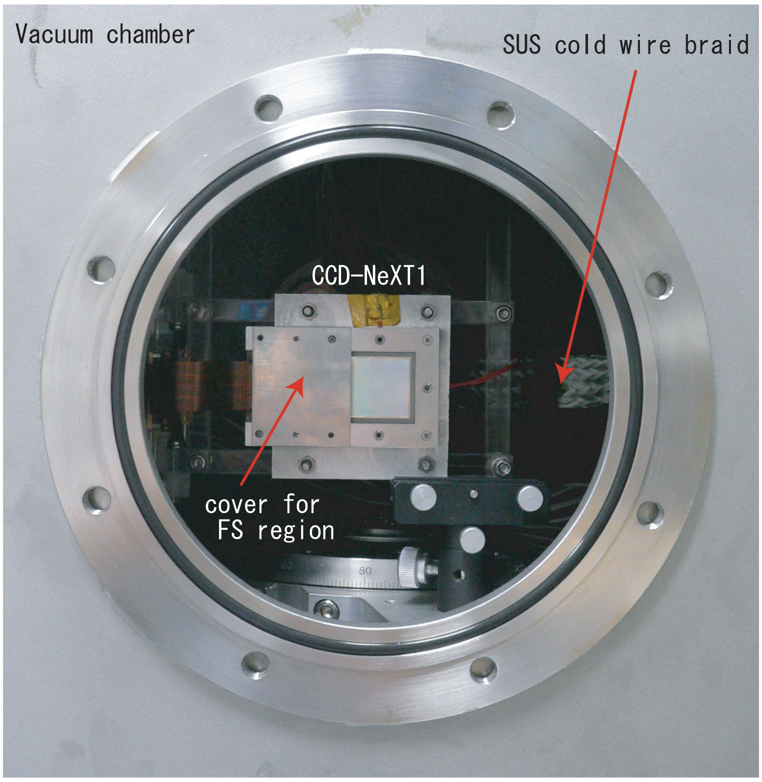


Figure 5.10: Picture of CCD-NeXT1 mounted in the large chamber system. The CCD-NeXT1 is joined to the cold head of Pulse Tube Cryocooler via a SUS flex wire braid. X-rays enter the CCD-NeXT1 in a direction perpendicular to the paper. In order to block the entrance of X-rays during transfer, the frame stored area (FS) of the CCD-NeXT1 is covered with a thick Al plate.

Chapter 6

Development I -Back Supportless CCD-

We next describe the development of a new-type CCD device for the SXI onboard the *NeXT* satellite. Since the SXI will be one of the main focal plane detectors for the HXT, focusing hard X-rays up to 60$\sim$80 keV with an unprecedented large effective area, the SXI is required to achieve (1) high sensitivity for X-rays and (2) the back-supportless structure for combining a hard X-ray detector. In order to produce such an unprecedented CCD, we programmed two plans, a "Baseline plan" and a "Goal plan", and advanced the development of the new CCDs in parallel. Details of these plans are described in chapter 4.

6.1 Baseline Plan

6.1.1 Development Plan

As described in chapter 4, we have already developed the Nch CCDs as "CCD-CREST" and "MAXI-CCD", which have shown excellent performance ([4, 37, 44, 63] and references there in). By removing the package and thinning down the CCD chip, we fabricated the small-size (12×12 mm^2) test device of BS-CCD. The main purpose of this fabrication is to examine (1) whether the thinning process and fabrication could be performed as we expected, and (2) whether the thinning process yields any performance degradation.

6.1.2 Fabrication of BS-CCD

For the fabrication of the BS-CCD, two characteristics are required; (1) In order to satisfy the requirement of high sensitivity for hard X-rays, we need to enlarge the depletion layer as much as possible. (2) In order to satisfy the requirement to transmit undetected X-rays as much as possible, we need to remove the field-free region and package which are not sensitive to X-rays.

To create the test model of the BS-CCD, we employed the "Deep 2K2" wafer, which is used for the MAXI-CCD [42]. Among practical X-ray CCDs, the MAXI-CCD is an excellent CCD, achieving good energy resolution, high detection efficiency, and low dark current. If there is no deterioration in the performance due to the thinning of the wafer, the test model of the BS-CCD is expected to achieve good performance equivalent to that of the MAXI-CCD.

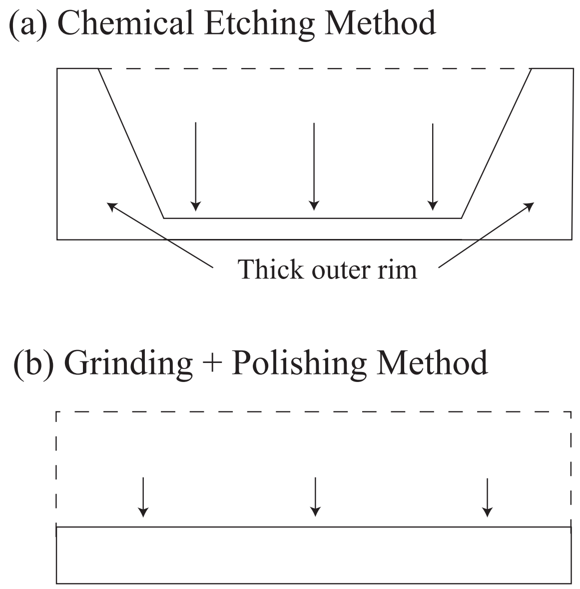


Figure 6.1: Schematic view of (a) the chemical etching method and (b) the grinding + polishing method.

We examined the method for the thinning of the wafer. To thin down the wafer to ~ 80 μm, equivalent to the thickness of the depletion layer, the thick rim area is required to maintain the strength of the chip and to handle the chip safely. In other words, we are required to process the chip in a concave shape (see Figure 6.1a). In this case, we need to use chemical etching, however, the resistivity of this wafer is too high to control the thickness as required. Therefore, we cannot apply this method for the Deep 2K2 wafer.

For the above reason, we decided to thin the wafer by grinding and polishing. This mechanical method is available independent of the resistivity of the wafer. The typical precision of thickness by the grinding and polishing processes are ± 15 μm and ± 5 μm, respectively. The typical roughness is 5 μm or less after both polishing processes. However, this method cannot process wafers with complicate shapes, such as the concave shape (see Figure 6.1b). We decided to thin the wafer to 200 μm from the viewpoint of the safe handling, though it could be processed more thinly. Thus, we thinned the Deep 2K2 wafer to 200 μm by this method. The flatness was about 17 μm within the size of 10 mm $\times$ 10 mm, which is the test model of the

BS-CCD (see below). Using this thinned wafer and the special package removed the backside, we assembled the test model of BS-CCD.

6.1.3 Performance of BS-CCD

6.1.3.1 Test model

P15 6-5B1P-2 (Deep1) First, we fabricated the BS-CCD using the "Deep1" wafer. Deep1 is one of the most well-informed wafers and is employed in many CCDs fabricated in HPK. Though Deep1 has the disadvantage in that the depletion layer needs to be enlarged because of its relatively lower resistivity compared to Deep2K2 used in CCD-CREST and MAXI-CCD, Deep1 was employed by the test device only to evaluate the effect of the thinning of the backside. We show the specification of this device in Table 6.1.

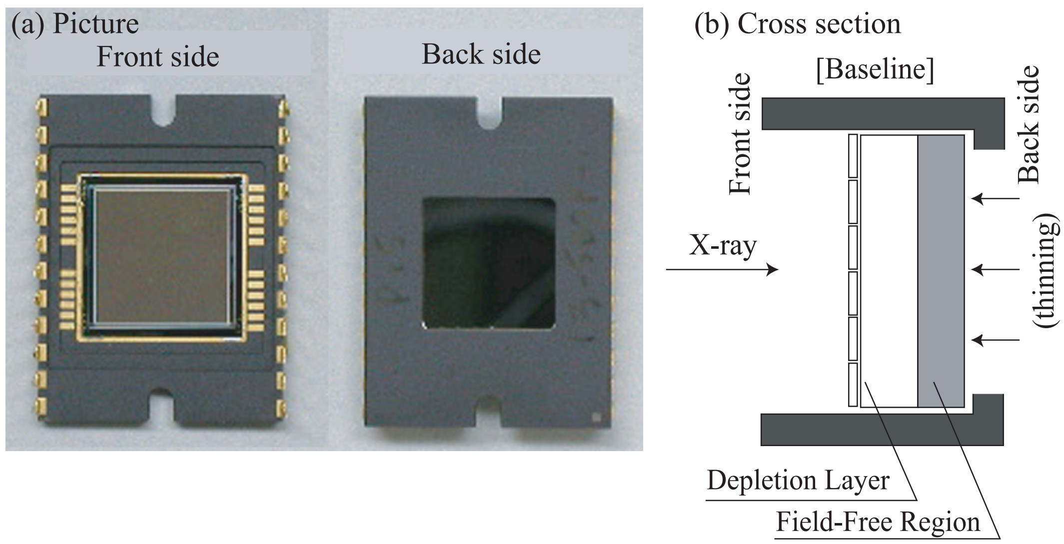


Figure 6.2: (a) Picture of the test model of BS-CCD. Due to the back supportless structure, the gate structure and the surface of the field-free region are exposed. (b) Schematic view of the test model of BS-CCD.

Figure 6.2 shows a photograph and a schematic view of the test model of BS-CCD. Due to the back-supportless structure, the gate structure and the surface of field-free layer are exposed. We show the results of the performance evaluation test in Table 6.1. We confirmed that this device drove normally and successfully detected incident X-rays. Figure 6.3 shows the spectrum of ^{55}Fe and ^{241}Am accumulating grade 0, 2, 3, 4, 6 events[1] . Though the readout noise of ~ 35 e^{-} seems to be bad, it is mainly attributed to the noise of the clock generator and the readout circuit

[1] The grade 0, 2, 3, 4, and 6 events are conventionally judged to be valid X-ray events in X-ray astronomy [46].

at Kyoto University (see also section 5.1), and not to that of the device itself. As described in the following paragraph, we have already confirmed that a CCD whose readout noise is equivalent to this device shows good readout noise (~ 7 e$^-$) when evaluated by the low-noise readout system at Osaka University[38].

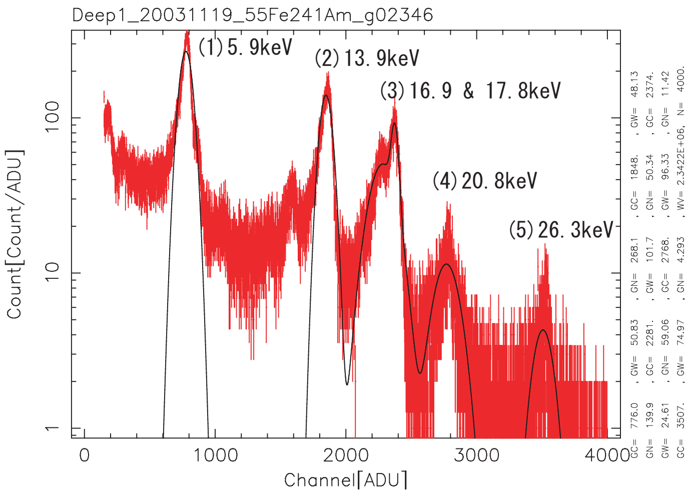


Figure 6.3: Spectrum of ^{55}Fe and ^{241}Am detected by BS-CCD of P15 6-5B1P-2 (Deep1). Grade 0, 2, 3, 4, and 6 events are accumulated.

We also found that the dark current and the CTI were < 0.1 e$^-$/sec/pixel, and 1.0×10^{-6} (horizontal) and 7.0×10^{-6} (vertical). These are essentially consistent with those of the unthinned CCDs, for example CCD-CREST and MAXI-CCD. From these results, we confirmed that there is no problem in the process of thinning of the backside.

Table 6.1: Specification and performance of test models of BS-CCD

Type No.		P15 6-5B1KF	P15 14-5B1P	KF201 17-5B1KF	KF201 21-5B1KF
Format		512 × 512			
Pixel size		24 μm × 24 μm			
Clock phase		2 phase			
Transfer method		Full Frame Transfer			
Illuminated method		Front Illuminated			
Wafer Type		Deep1(4inch)	Deep2K2(4inch)	Deep5(6inch)	
Readout noise	[e$^-$(rms)]	-	7*	-	-
		35	36	42	30
Energy resolution	[eV(FWHM)]	-	140** (@5.9keV)	-	-
		570 (@5.9keV)	670 (@22.2keV)	850 (@22.2keV)	610 (@22.2keV)
Dark current	[e$^-$/pixel/sec]	<0.1 (-110degC)	<0.1 (-110 °C)	<0.1 (-73 °C)	0.1 (-73 °C)
Node sensitivity	[μV/e^-]	-†	2.3	1.8	2.6
CTI (vertical)	[10^{-6}/transfer]	7.0	2.1	9.3	36
CTI (horizontal)	[10^{-6}/transfer]	1.0	1.9	2.3	6.3
Depletion layer	[μm]	10(ratio)	65	76	73
Wafer	[μm]	200‡	190	-(not thinned)	-(not thinned)

* read-out noise measured by Osaka University group.

** energy resolution measured by Osaka University group.

† (not measured).

‡ nominal value reported by HPK (not measured).

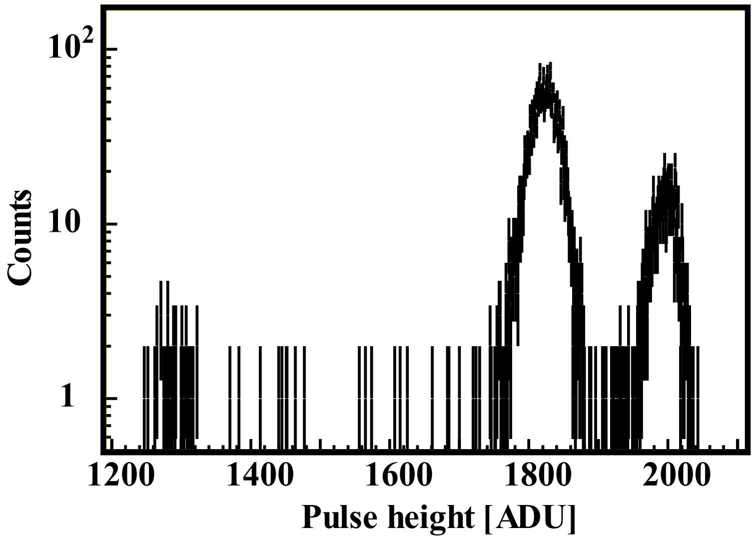


Figure 6.4: Spectrum of ^{55}Fe detected by BS-CCD of P15 14-5B1P-4 (Deep2K2). This data is obtained with $E \sim NA$ system of Osaka University. Single pixel events (grade 0) are accumulated.

P15 14-5B1P-4 (Deep2K2) Based on the successful results described in the previous paragraph, we fabricated BS-CCD on the Deep2K2 wafer, which is expected to achieve a thick depletion layer of $\sim$ 80 μm. We show the specification of this device in Table 6.1. The appearance of this device is the same as P15 6-5B1P-2 (see Figure 6.2).

Figure 6.4 shows the spectrum of ^{55}Fe obtained by this BS-CCD, accumulating single pixel (grade 0) events. This data is obtained with the $E \sim NA$ system of Osaka University [38]. The readout noise of this system is significantly lower than that of the readout system of Kyoto University. Mn K_α (5.9 keV) and Mn K_β (6.5 keV) lines are clearly separated. The readout noise and energy resolution are 7 e^- and 144 eV at 5.9 keV (Mn K_α), respectively. These are excellent and essentially equivalent to those of MAXI-CCD.

We also evaluated this device using our readout system. Though the readout noise of our system is higher than that of the $E \sim NA$ system of Osaka University, it is useful to compare the characteristics of P15 6-5B1P-2 (Deep1) and this device evaluated in the same experimental setup. Figure 6.5 and 6.6 show the X-ray image and spectrum of ^{109}Cd detected by this device, respectively. The readout noise is 36e^-, which is same as that of P15 6-5B1P-2. Therefore, the readout noise of P15 6-5B1P-2 (Deep1) itself might also be the same as this device. The dark current and CTI are also equivalent to those of P15 6-5B1P-2 (Deep1).

Using the well-calibrated X-ray source of ^{109}Cd (see section 5.2.1), we measured the detection efficiency of the BS-CCD and estimated the thickness of its depletion

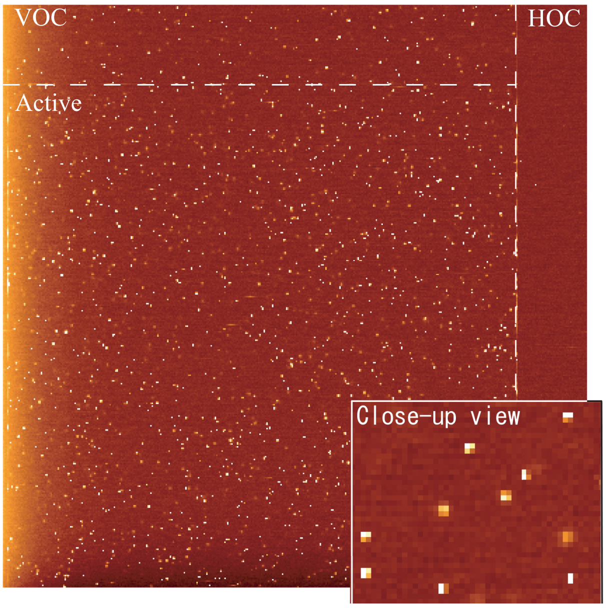


Figure 6.5: Acquired image of ^{109}Cd detected by BS-CCD of P15 14-5B1P-4 (Deep2K2).

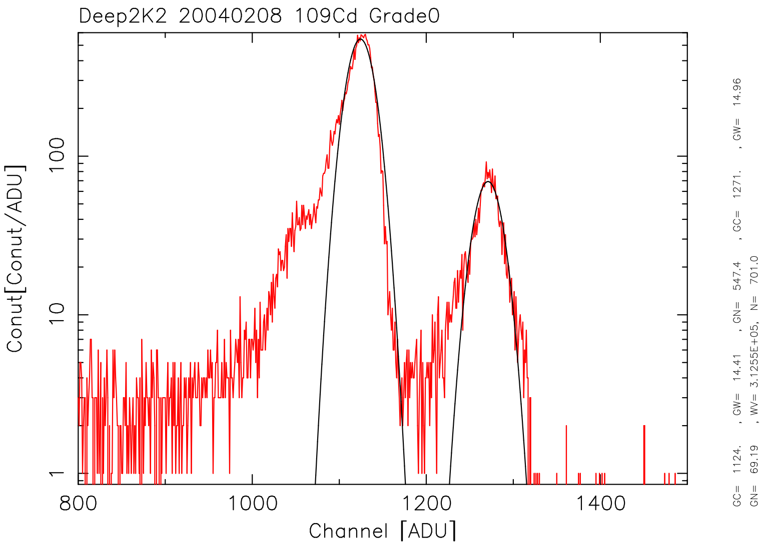


Figure 6.6: Spectrum of ^{109}Cd detected by BS-CCD of P15 14-5B1P-4 (Deep2K2). Single pixel events (grade 0) are accumulated.

layer. We accumulated X-ray events of grades 0, 2, 3, 4, and 6 and found the detection efficiency to be 4.1% at 22.2 keV (Ag K_α). This detection efficiency is equivalent to that of the 65 μm-thickness depletion layer, which is essentially consistent with the thickness of the depletion layer expected from the resistivity of the Deep 2K2 wafer. We also measured the transmissivity of the BS-CCD with ^{109}Cd. The transmissivity of 87 % (at 22.2 keV) is equivalent to that of the 190 μm-thickness Si wafer. This thickness is consistent with our designed value.

Based on these results, we confirmed that there was no degradation in the performance of the BS-CCD compared to that of the unthinned CCD as MAXI-CCD; in addition, no problems were found in the process of thinning of the backside.

KF201 17-5B1KF-5 (Deep5) As shown in the previous paragraph, we successfully developed the test model of BS-CCD. We judged that we have already learned the process of manufacturing BS-CCD with a p-type semiconductor. Considering the future demand for the production of large-size CCD as the flight model onboard $NeXT$, we changed the size of the Si wafer from a 4-inch radius to a 6-inch radius. We could obtain 6-inch radius wafers (6-inch wafers) with quality as good as that of the 4-inch radius wafers (4-inch wafers). However, the manufacturing line had to be changed with the change in the wafer size, and so it was necessary to confirm whether the CCDs fabricated on the 6-inch wafer show equivalent characteristics as those on the 4-inch wafers. We experimentally manufactured front-illuminated CCDs with a 6-inch high-resistivity wafer, named "Deep5", which is equivalent to the Deep2K2 wafer. As shown in Table 6.1, the format is the same for the test model of BS-CCD as P15 6-5B1P-2 (Deep1) and P15 14-5B1P-4 (Deep2K2). However, as shown in Figure 6.7, the structure of this device was not a back-supportless structure, meaning that we did not thin the backside of this wafer and the backside of the package was not removed.

In the inspection of this device before shipment, performed by HPK, the characteristics of this device were found to be essentially equivalent to those of the CCDs fabricated on 4-inch wafers, however, the dark current was reported to be 565 e^-/sec/pixel at -20 °C, which is $\sim$ 10 times higher than that of the CCDs fabricated on 4-inch wafers (Deep2K2). We evaluated this device paying special attention to the behavior of the dark current at low temperatures. The readout noise, CTI, and the thickness of the depletion layer are equivalent to those of Deep2K2 CCD, as reported earlier. The dark current is also equal to that of the Deep2K2 CCD at a sufficiently low temperature. The results are shown in Table 6.1. The reason for the high dark current at high temperatures is unknown. However, we judged the Deep5 wafer and the manufacturing process for the Deep5 CCD had no problems because the dark current was sufficiently low (< 0.1 e^-/sec/pixel) at the standard temperature (< -70 °C) for driving X-ray CCDs.

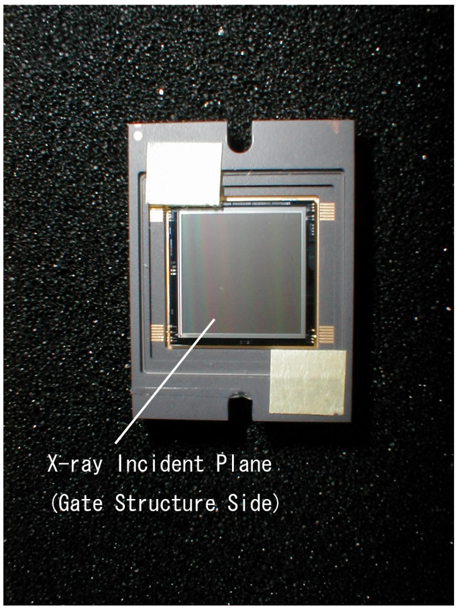


Figure 6.7: Picture of the test model of the CCD fabricated on a 6-inch wafer.

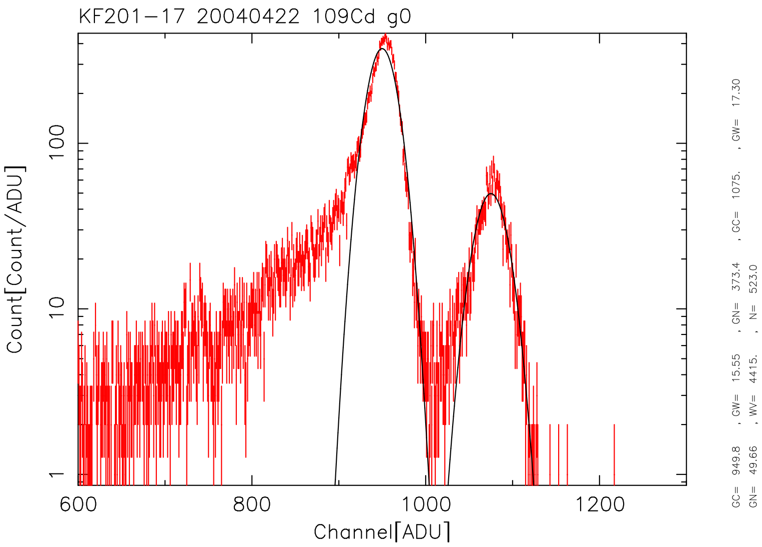


Figure 6.8: Spectrum of ^{109}Cd detected by BS-CCD of KF201 17-5B1KF-5 (Deep5). Single pixel events (grade 0) have accumulated.

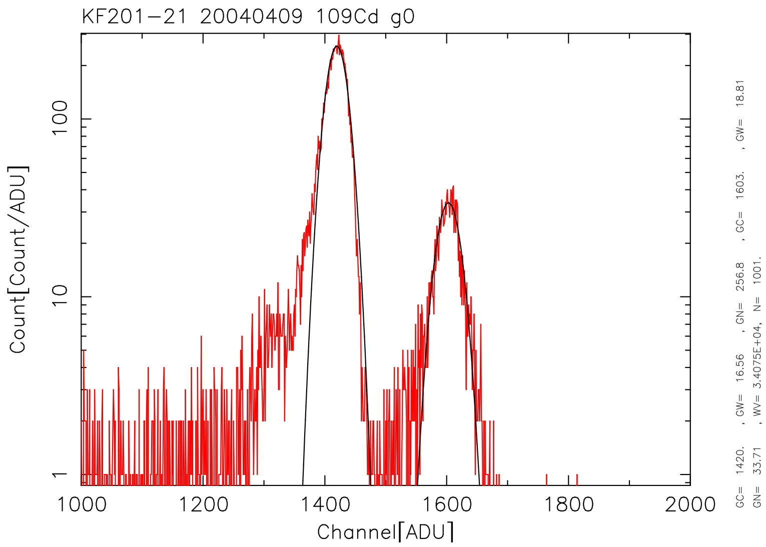


Figure 6.9: Spectrum of ^{109}Cd detected by the BS-CCD of KF201 21-5B1KF-5 (Deep5). Single pixel events (grade 0) have accumulated.

KF201 21-5B1KF-11 (Deep5) This device is also fabricated on the Deep5 wafer in the same manufacturing line as the KF201 17-5B1KF-5. The format and appearance are entirely the same as those of KF201 17-5B1KF-5. Though this device also showed a high dark current of 1487e$^-$/sec/pixel at -20 °C, we confirmed that this decreased to < 0.1e$^-$/sec/pixel at a temperature of -76 °C. As shown in Table 6.1, the characteristics are essentially equivalent to those of KF201 17-5B1KF-5. We confirmed that the fabrication process with the new manufacturing line had no problem.

6.1.3.2 Prototype of hybrid detector

To demonstrate the characteristics of the BS-CCD, we combined the BS-CCD and the CdTe detector (commercially available). The CdTe detector used in these experiments is the XR-100T-CdTe produced by Amptek Inc. As shown in Figure 6.10a, the arrangement of the detectors are the same as that in the WXI. We irradiated with X-rays of ^{241}Am from above these devices.

First, we detached the BS-CCD and obtained the spectrum of ^{241}Am using only the CdTe detector (see Figure 6.10b). Thus, the X-rays from the ^{241}Am entered the CdTe detector directly. The exposure time was 300 sec. We show the observed intensity of each line in the raw C^{off}_{CdTe} in Table 6.2. From 10 keV to 60 keV, the efficiency of this detector is almost 100%, therefore the ratio of C^{off}_{CdTe} represents the intensity ratio of each line from ^{241}Am.

Secondly, as shown in Figure 6.10a, we set the BS-CCD above the CdTe detector. Figure 6.10c and 6.10d show the spectra obtained with the BS-CCD and the CdTe detector placed under the BS-CCD. The total exposure time of the BS-CCD and the CdTe detector were 600 sec and 300 sec, respectively. The spectrum shown in Figure 6.10c accumulated events of grades 0, 2, 3, 4, and 6. We show the line intensity of each line seen in Figure 6.10c (by the BS-CCD) and 6.10d (by the CdTe detector) in the rows C_{CCD} and C^{on}_{CdTe} in Table 6.2, respectively.

To verify the above results of the thickness of the wafer (d_{WF}) $\sim$ 190 μm, we calculated the transmissivity ($C^{on}_{CdTe}/C^{off}_{CdTe}$, see Table 6.2) at the energy of each line and compared it with the expected transmissivity of the Si wafer of 190 μm thickness. As shown in Figure 6.11, these are approximately consistent with each other. This also demonstrates that almost all the hard X-rays pass through the BS-CCD wafer and are detected by the CdTe detector.

We also verified the results of the thickness of the depletion layer (d_{DL}) $\sim$ 65 μm. Since the size of the imaging area of the BS-CCD is different from that of the CdTe detector, C_{CCD}/C^{off}_{CdTe} does not indicate the detection efficiency of the BS-CCD. However, the ratio of C_{CCD}/C^{off}_{CdTe} of each line is equal to that of the detection efficiency at the energy of each line. Therefore, we estimated the detection efficiency of the BS-CCD (Q_{CCD}) at the energy of each line by normalizing C_{CCD}/C^{off}_{CdTe} at 13.9 keV to 0.17 equal to the detection efficiency of the 65 μm-thick depletion layer, *i.e.*, $Q_{CCD} = C_{CCD}/C^{off}_{CdTe} \times 0.17/1.09$ (see also Table 6.2). As shown in Figure 6.11, we plotted the estimated detection efficiencies (Q_{CCD}) and confirmed they were consistent with the expected detection efficiencies of the 65 μm-thickness depletion layer.

Table 6.2: Intensities of the lines of ^{241}Am, transmissivity and estimated detection efficiency of BS-CCD

		Line Energy [keV]								
Detector		13.9	16.9	17.7	20.8	26.2	32.1	33.3	36.4	59.6
CdTe (without CCD)	C^{off}_{CdTe} †	9655	12071	5856	4871	2459	993	684	1876	30493
CdTe (with CCD)	C^{on}_{CdTe} †	5475	9275	4288	4164	2315	1047	760	1856	30739
	$C^{on}_{CdTe}/C^{off}_{CdTe}$	0.57	0.77	0.73	0.85	0.94	1.05	1.11	0.99	1.01
CCD	C_{CCD} †	10552	9897		1559	392	-	-	-	-
	C_{CCD}/C^{off}_{CdTe}	1.09	0.55		0.32	0.16	-	-	-	-
	Q_{CCD} ††	0.17	0.086		0.052	0.025	-	-	-	-

†: Total counts of each line [counts]. ††: $Q_{CCD} = C_{CCD}/C^{off}_{CdTe} \times 0.17/1.09$.

6.1.3.3 Evaluation model -CCD-NeXT1-

Based on these successful results, we started to fabricate the developed BS-CCD device as “CCD-NeXT1”. This device is characterized as an evaluation model of

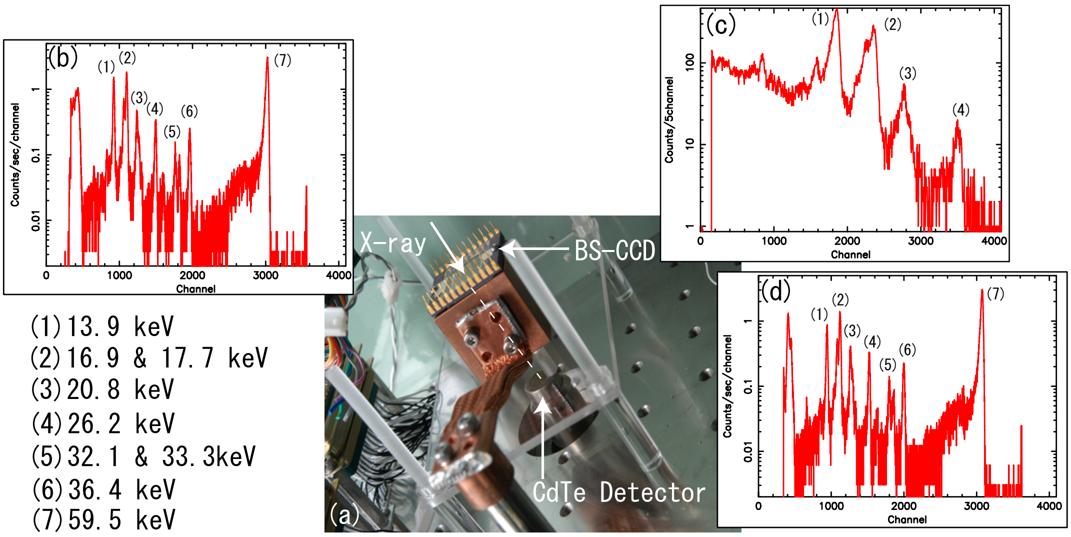


Figure 6.10: (a) Photograph of the test model of the WXI. (b)^{241}Am spectrum acquired by the CdTe detector. There is no barrier between ^{241}Am and the detector. (c) Spectrum of ^{241}Am acquired by the BS-CCD. Grades 0, 2, 3, 4, and 6 events have accumulated. (d) Spectrum of ^{241}Am acquired by the CdTe detector placed under the BS-CCD. X-rays penetrating the BS-CCD are detected.

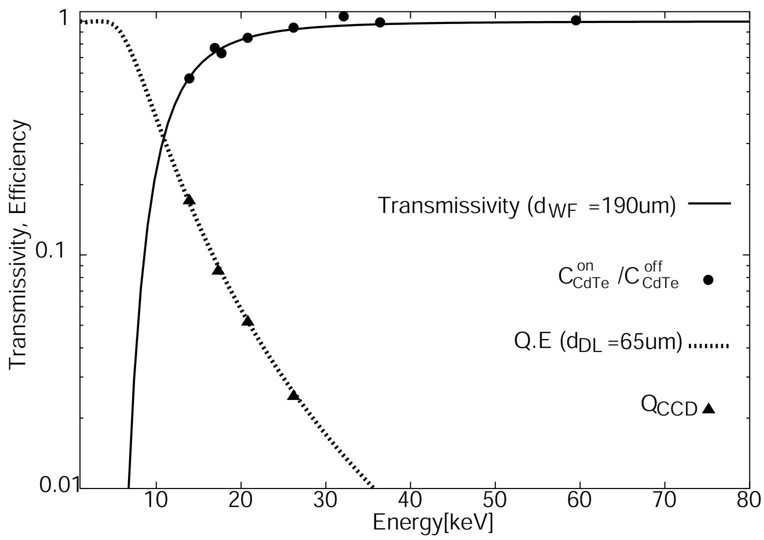


Figure 6.11: Transmissivity and detection efficiency (Q .E.) of the BS-CCD. The solid and dotted lines show the expected transmissivity of 190 μm-thick Si wafer and the expected detection efficiency of the CCD with a 65 μm-thick depletion layer, respectively. The solid circles and triangles show the observed transmissivity ($C^{on}_{CdTe}/C^{off}_{CdTe}$) and the estimated detection efficiency (Q_{CCD}), respectively (see Table 6.2).

the baseline-plan SXI (see Table 4.3 in chapter 4).

Making use of the experience of developing domestic CCDs of CCD-CREST, MAXI-CCD, and the test model of BS-CCD, as described previously, we attempted to produce the CCD-NeXT1. The format and pixel size were 2000 pixels and $12\mu\mathrm{m} \times 12\mu\mathrm{m}$, which are the same as those of the CCD-CREST2. The charge transfer method is the frame transfer. We show a picture of the CCD-NeXT1 in Figure 6.12.

The wafer was thinned down to 150 μm. Though we adopted the grinding and polishing method for thinning the wafer in the case of the test model, this wafer was thinned by only grinding. The reason for omitting the polishing process is that physical destruction frequently occurs in this process. Many microscopic trails are apparently present on the ground surface only due to the grinding method. We show a close-up view of the ground surface of the CCD-NeXT1 in Figure 6.13. We can see many tiny trails along the direction of the grinding. We observed these trails closely using a color laser three-dimensional profile microscope (VK-9500; Keyence, Osaka, Japan). Figure 6.14 shows the surface condition on the grinding surface. We found the depth and the width to be $\sim 0.3\mu$m peak-to-peak and sub-μm, respectively. Compared to the thickness of the wafer ($\sim 150\mu$m) and the size of the pixels ($\sim 12\mu$m), they are negligibly small. Therefore, we made a judgment that it is not a problem to omit the polishing process. In the following, the thinning of the wafer is performed only by the grinding method.

KG103 9-20A0KG-2 KG103 9-20A0KG-2 is fabricated on the Deep1 wafer thinned down to 150 μm by the grinding method. We measured the thickness of the wafer in this device. As shown in Figure 6.15, we set the IA of the CCD-NeXT1 between the sealed radio isotope of ^{241}Am and the CdTe detector, and acquired an "absorbed" ^{241}Am spectrum shown in the blue curve in Figure 6.16. Subsequently, we detached CCD-NeXT1 and acquired an "un-absorbed" spectrum (the red curve in Figure 6.16) under the same experimental arrangement. The intensity ratio of each characteristic X-ray line between the absorbed and unabsorbed spectra shows the transmissivity (T_{CCD}) of this wafer. We calculated the absorptivity A_{CCD} $(1 - T_{CCD})$ at each characteristic X-ray line and compared the expected A_{CCD} for X-rays absorbed by silicon with 150-μm thickness. As shown in Figure 6.16, they are approximately consistent.

KG103 22-20A0KG-2 We evaluated the performance of KG103 22-20A0KG-2. This device was fabricated on the Deep5 wafer. The performance test for this device was performed using the setup described in section 5.2.2. We irradiated X-rays from ^{55}Fe over the whole area of CCD-NeXT1 uniformly. As described in section 5.2.2, the frame stored area is covered by a thick Al plate. The CCD-NeXT1 was driven by the frame transfer method in this evaluation. The results are shown in Table 6.3. Figure 6.17 (left) shows the acquired spectrum of ^{55}Fe with accumulated grade 0

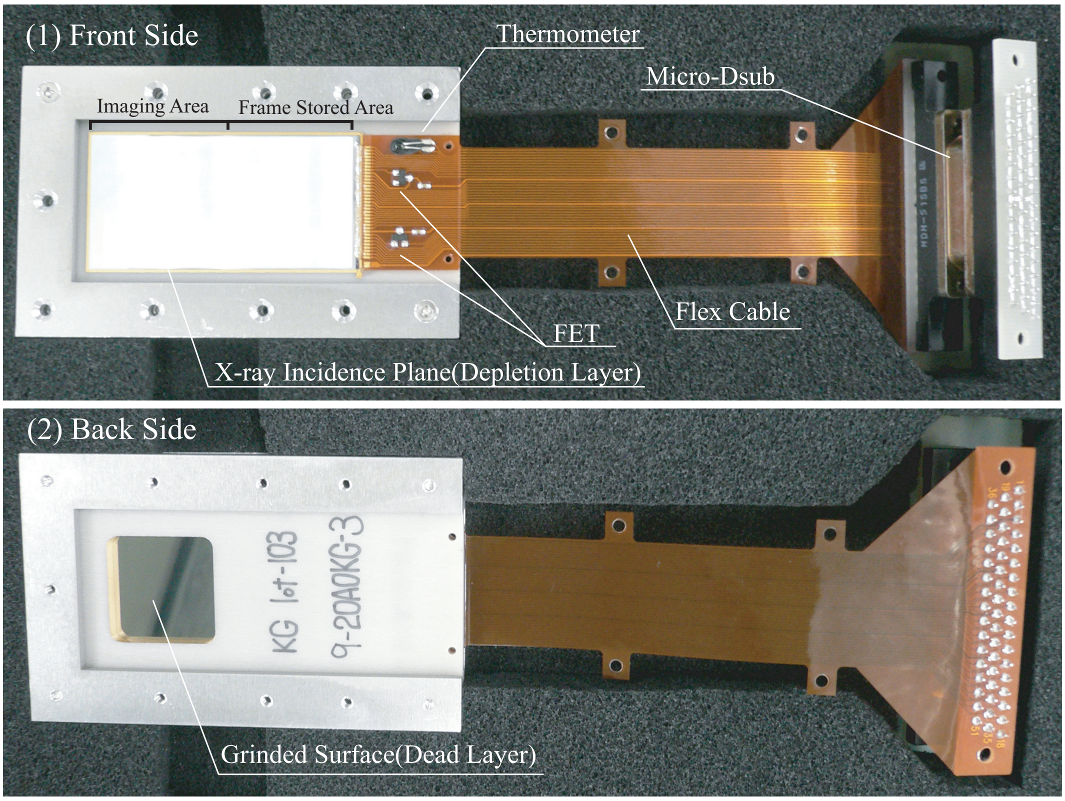


Figure 6.12: Picture of the CCD-NeXT1. (1) Front side. (2) Back side. Due to the presence of the Al coating, we can clearly see that the reflection forms on the surface of both sides.

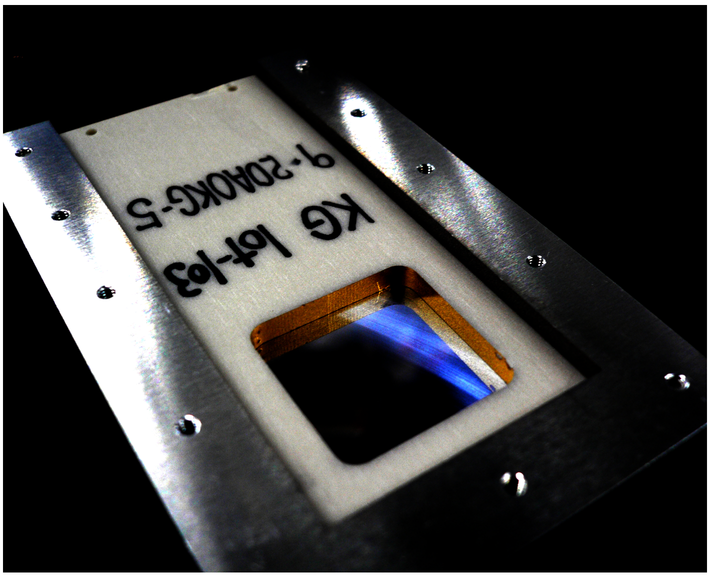


Figure 6.13: Tiny trails found on the grinding surface of the CCD-NeXT1. We adjusted the color of the picture in order to clearly show these trails.

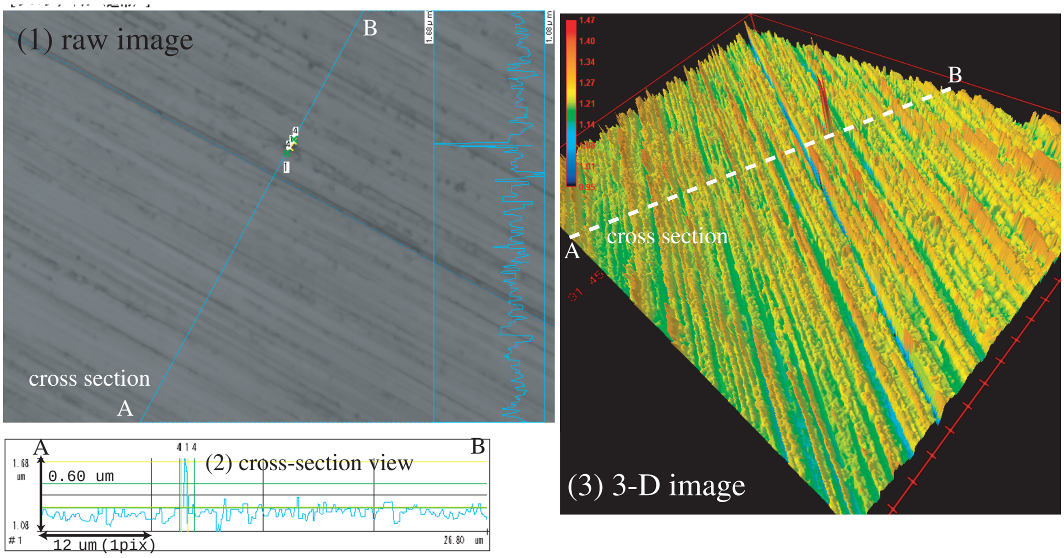


Figure 6.14: Surface condition of the ground wafer measured by a color laser three dimensional profile microscope (VK-9500; Keyence, Osaka, Japan). (1) Raw image of a part of the ground surface. (2) Cross-sectional view acquired by laser ranging. (3) 3-D view.

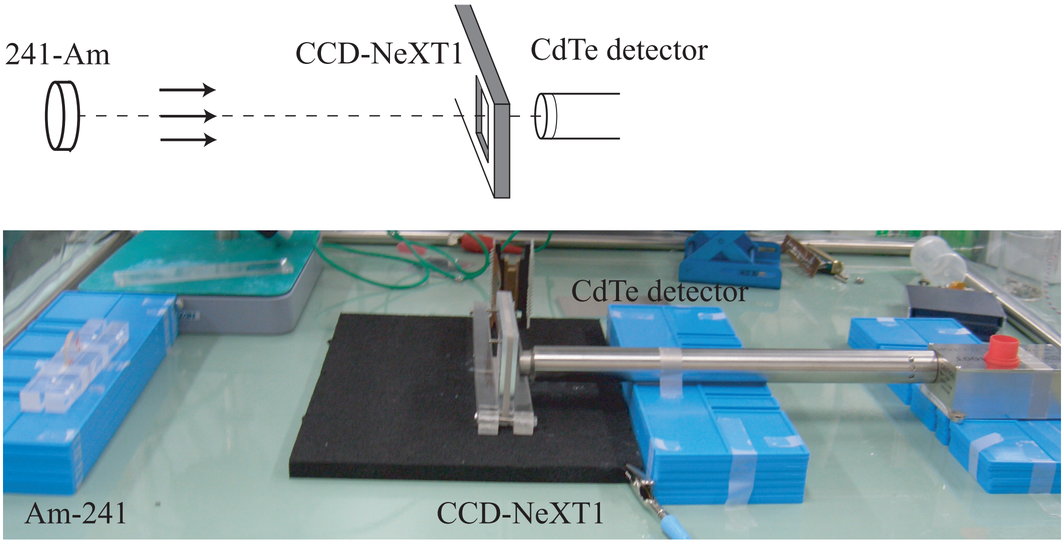


Figure 6.15: Experimental setup for measurement of the thickness of the wafer of CCD-NeXT1 (KG103 9-20A0KG-2). We set the imaging area of CCD-NeXT1 between the sealed radio isotope of ^{241}Am and the CdTe detector.

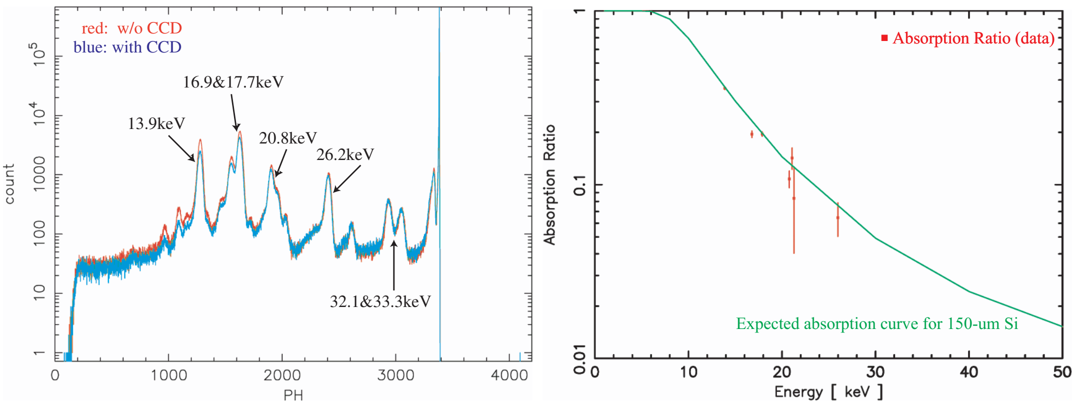


Figure 6.16: (left) Spectra of ^{241}Am detected by the CdTe detector. The red line shows the spectrum obtained without CCD-NeXT1 between the radio isotope ^{241}Am and the CdTe detector. The blue line shows the absorbed spectrum by the IA of CCD-NeXT1 (KG103 9-20A0KG-2). (right) The absorptivity at each characteristic X-ray line between the absorbed spectrum and the unabsorbed one. A solid curve represents the expected absorptivity in the case where the thickness of the IA of CCD-NeXT1 is 150 μm.

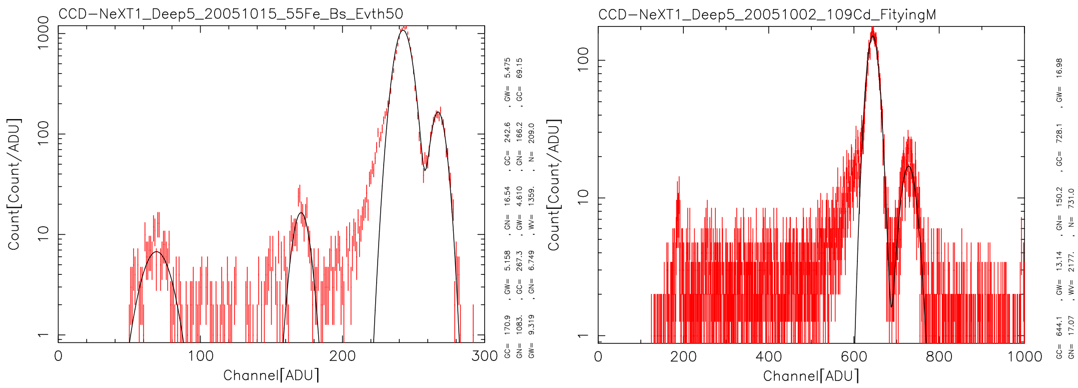


Figure 6.17: Spectrum of ^{55}Fe (left) and ^{109}Cd (right) detected by the CCD-NeXT1 of S/N KG103 22-20A0KG-2

events. The readout noise and energy resolution were 21e$^-$ and 299 eV at the 5.9 keV line. Though the read-out noise of 21 e$^-$ appears to be bad, it is mainly attributed to the noise of the clock generator and the readout circuit of Kyoto University (see also section 5.1). The node sensitivity of 3.2 μV/e$^-$ is higher than those of the test device, therefore the read-out noise of CCD-NeXT1 itself is expected to be < 7 e$^-$, which is the same as that of P15 14-5B1P-4 measured by Osaka University (see Table 6.1). The CTI of 1.5×10^{-6} (vertical) and 1.2×10^{-6}/transfer (horizontal) is also as good as that of the test device.

Table 6.3: Specification and performance of CCD-NeXT1

Type No.	KG103 22-20A0KG-2 (Front Illumination)	
Number of pixels	$2000 \times 2000 \times 2^{\dagger}$	
Pixel size	12 μm $\times$ 12 μm	
Clock phase	2 phase	
Transfer method	Frame Transfer	
Readout noise (rms)	21 e$^{-\ddagger}$	
Energy resolution (FWHM)	300 eV (at 5.9keV)	
Dark current	12e$^-$/pixel/hour (at -77 °C)	
Thickness of the depletion layer	84 μm	
Thickness of the wafer	625 μm	(not thinned)
Node sensitivity	3.2 μV/e^-	
CTI (vertical)	1.5×10^{-6}/transfer	
CTI (horizontal)	1.2×10^{-6}/transfer	

† Sum of imaging area and frame stored region.

‡ Most of this value is thought to originate in the system noise.

We measured the thickness of the depletion layer with the well-calibrated X-ray source of ^{109}Cd. Details of the experimental setup are described in section 5.2 In this measurement, 75 % of the ^{109}Cd events are grade 7 events, which are conventionally classified as background events. This value is very large compared to the grade 7 ratio (8%) of the test device KF201 21-5B1KF-11 fabricated on the same Deep5 wafer. This is caused by the small pixel size (12μm $\times$ 12μm) of CCD-NeXT1 which is half the size of that of the test devices. To help in our understanding, we show the cross-section of a CCD chip and the appearance of charge distribution on the surface of a CCD in Figure 6.18. When the pixel size becomes half, the charge cloud spreads out over two times more number of pixels in appearance.

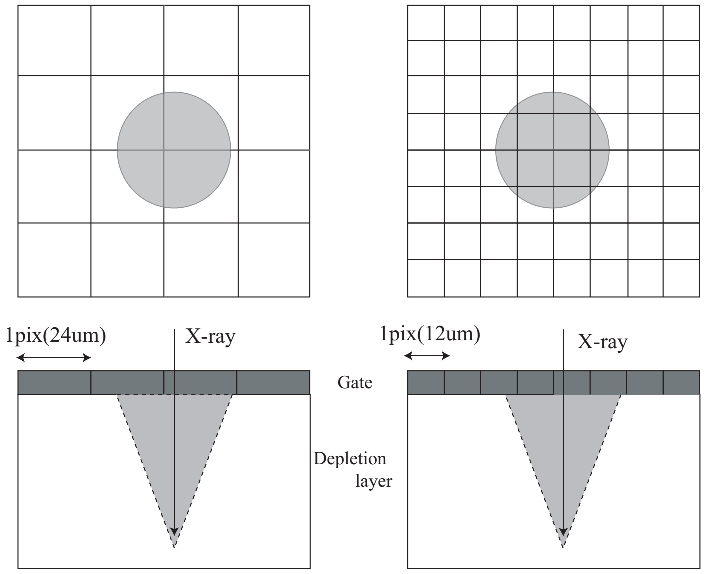


Figure 6.18: The cross-section of a CCD chip and the appearance of the charge distribution on the surface of the CCD

Therefore, we consider that most grade 7 events are also valid X-ray events in this evaluation test. To confirm this speculation, we made image files binned 2 $\times$ 2 pixels in one pixel (2 $\times$ 2 binned image). We analyzed these binned image files again using the grading method, and found that the ratio of grade 7 decreased from 75% to 15%. This results shows that the conventional grade method should be applicable to CCDs which have a pixel size of 24μm $\times$ 24μm, but it is difficult to apply to those with a pixel size of 12μm $\times$ 12μm. We then reconstructed the ^{109}Cd events by the fitting method. As described in section 3.6.2, the fitting method is applicable regardless of the size of the events. We show the obtained ^{109}Cd spectrum in Figure 6.17 (right).

The detection rate of ^{109}Cd is 0.14 count s^{-1}, which corresponds the detection efficiency of 5.2 %. This detection efficiency is equivalent to that of the 84-μm thickness of the depletion layer as we expected.

6.1.4 Summary of baseline plan

We summarize the development of the Nch CCD for the BS-CCD following the baseline plan;

- We developed the BS-CCD for the Wideband X-ray Imager onboard the NeXT satellite.
- We built the test model of the BS-CCD using Deep 2K2 , the same wafer as MAXI-CCD. We confirmed that the thickness of the wafer and the depletion layer are 190 μm and 65 μm, respectively.
- The performance of the test model of the BS-CCD was comparable to that of MAXI-CCD. The energy resolution at 5.9 keV is 144 eV and the read-out noise is 7 e^- (r.m.s.).
- Based on these successful results, we built the evaluation model of the BS-CCD as the "CCD-NeXT1". This device also shows good performance, essentially equivalent to that of the test model of the BS-CCD.

6.2 Goal Plan

As shown in the previous section, we successfully developed the Nch BS-CCD which has a thicker depletion layer ($\sim$ 80 μm) and a thinner field-free region ($\sim$ 70 μm) compared with established X-ray CCDs. However, in the process of developing the Nch BS-CCD, we found some inevitable problems: (1) the thickness of the depletion layer was limited to within $\sim$ 80 μm primarily because a wafer with above 5k $\Omega \cdot$ cm-resistivity was not available, and (2) the thickness of the silicon wafer cannot be thinned to 150 μm-thickness from the view-point of safe handling and mechanical strength. In the goal plan, we aim to significantly increase the thickness of the depletion layer by employing a Pch CCD.

6.2.1 Development Plan

The advantages of the Pch CCD are that (1) high sensitivity for **hard** X-rays can be essentially acquired by thickening the depletion layer, and (2) high sensitivity for **soft** X-rays can be acquired by using the back-illuminated structure. Furthermore, we note that the characteristics (1) and (2) can be compatible, and we aim to realize the "perfect" back-supportless structure using the fully-depleted wafer. However, because the experience of developing the Pch CCD is very poor, we need to advance its development gradually. As described in chapter 4, we participated in the development of the Pch CCD conducted by NAOJ and shared in the performance evaluation examinations of the test device with a group of NAOJ. We performed the evaluation of test devices from the viewpoint of the X-rays detector and fed the results back to the development of the device in the following process;

(1) We developed devices which have a high sensitivity to hard X-ray photons. To achieve this goal, it is essential to increase the thickness of the depletion layer. We measured the sensitivity for hard X-rays of test devices fabricated on n-type semiconductor with high resistivity, and cleared up their performance problems.

(2) We developed devices which have high sensitivity to soft X-ray photons. To achieve this goal, it is essential to make the back-illuminated CCD. We verified that the thick depletion layer, already achieved in step (1), could be maintained and the performance does not degrade.

(3) Parallel to (1) and (2), we examined the basic characteristics of test devices. In particular, we checked problems with the gain of the amplifier and CTI in detail to realize good energy resolution for which to be one of the strong points of X-ray CCD.

6.2.2 Improvement in detection efficiency for hard X-rays

From Eq. (3.11), the thickness of the depletion layer (d_{DL}) essentially depends on the mobility of the major carrier (μ) and the resistivity of the Si wafer (ρ) for a given bias voltage(V), as indicated by the following equation,

$$d_{\mathrm{DL}} \propto \sqrt{\mu \rho V}. \tag{6.1}$$

In the Pch CCD, the major carrier is an electron whose mobility is a factor of three higher than that of a hole, which is the major carrier of the Nch CCD (see Figure 4.7). N-type silicon, used for the fabrication of the Pch CCD with very high resistivity of over $10\mathrm{k}\Omega \cdot \mathrm{cm}$, is available. On the other hand, the resistivity of the p-type silicon (ρ_{Nch}) used for the fabrication of the Nch CCD is limited to within $5\ \mathrm{k}\Omega \cdot \mathrm{cm}$. The above two features allow for the operation of the Pch CCD with a thickness of the depletion layer of 300μm without applying a high bias voltage.

6.2.2.1 test device

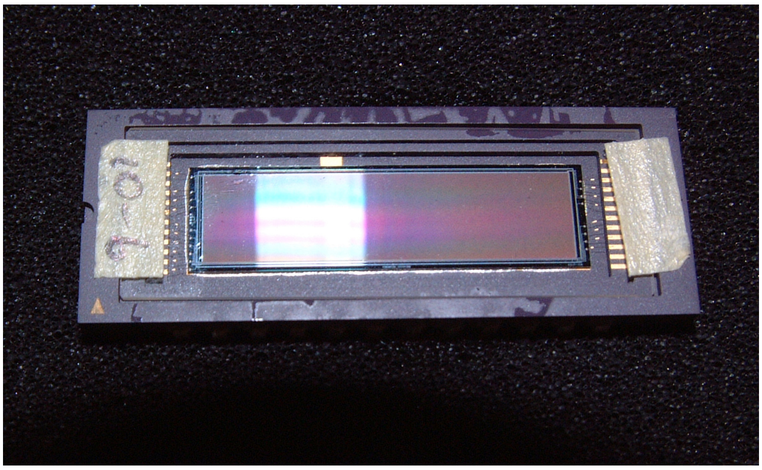


Figure 6.19: Overview of the front-illuminated Pch CCD (Pch3, 5, 8A, 14B). The pixel size is $24\mu\mathrm{m} \times 24\mu\mathrm{m}$ and the format is 1024×256 pixels.

Pch3 This device is a prototype of the Pch CCD fabricated on the existing silicon wafer to confirm the assembly method of the Pch CCD. Two kinds of prototypes were made in every material that a resistivity was different; the wafer resistivity of Pch 3-4 and Pch 3-10 is $1\mathrm{k}\Omega \cdot \mathrm{cm}$ and $6\mathrm{k}\Omega \cdot \mathrm{cm}$, respectively. We successfully drove these devices and detected X-ray photons. However, as shown in Figure 6.20, there are many apparent vertical stripes in the active area. These stripes reflect the imperfections in the charge transfer, and the lattice imperfections may be caused by the processing conditions and the wafer material. We plan to solve this problem by changing the wafer material and the optimization of the process conditions. We measured the detection efficiency of Pch 3-10 by using the collimated X-ray source of ^{109}Cd, which is described in section 5.2.1. The measurements of the X-ray detection efficiency of test devices described in the following are performed under essentially the same experimental setup unless otherwise noted.

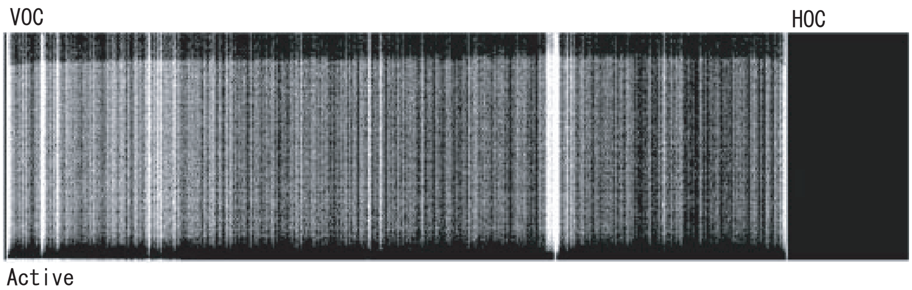


Figure 6.20: Acquired dark image with Pch 3-10. We see apparent vertical stripes which may be caused by a lattice imperfection.

As shown in Table 6.4, we confirmed that the detection efficiency of Pch 3-10 increases as we apply a higher gate voltage. We recorded a maximum detection efficiency of 7.7 % at the gate voltage of -12 V, which is equivalent to that of the depletion depth of 124 μm. These values are the same as expected, and the depletion depth of ~ 100 μm is thicker than any established Nch CCD fabricated on a p-type semiconductor.

Table 6.4: Comparison of the detection efficiency for ^{109}Cd detected with Pch 3-10 at various gate voltages

Gate voltage [V]	Q. E.* [%]	Depletion depth** [μm]
-2	5.6	89
-4	4.7	74
-6	6.4	103
-8	6.8	109
-12	7.7	124

$\star$: Detection efficiency at 22.2 keV (^{109}Cd K$_{\alpha}$). We reconstructed the spectrum by accumulating grade 0, 2, 3, 4, and 6.

$\star\star$: Thickness of depletion layer corresponds to detection efficiency.

Table 6.5: Specification and typical performance of test models of Pch CCD (Front Illumination)

Type No.		Pch 3-4	Pch 3-10	Pch 5-9	Pch 8A-7	Pch 14B-5
Format				1024 × 256		
Pixel size				24 μm × 24 μm		
Clock phase				2 phase		
Transfer method				Full Frame Transfer		
Illuminated method				Front Illuminated		
Wafer Resistivity		1k$\Omega \cdot$ cm	6k$\Omega \cdot$ cm	>10k$\Omega \cdot$ cm	>10k$\Omega \cdot$ cm	>10k$\Omega \cdot$ cm
Detection efficiency*	[%]	3.1	7.7	16.3	20.2	22.4
Depletion layer	[μm]	49	124	276	349	372

* Detection efficiency at 22.2 keV (^{109}Cd K$_\alpha$).

Pch5 We found that there was no big problem in the production process of the Pch CCD judging from the results of the performance evaluation of Pch 3-10. As the next step, we evaluated the test device of Pch 5-9 fabricated on a super high-resistivity (over 10k$\Omega \cdot$ cm) wafer which was newly obtained. We were able to successfully detect X-rays from ^{109}Cd. Figure 6.23 (left) shows the image of the detected events of ^{109}Cd. Most of them were classified as grade 7, spread out over 2 × 2 pixels. Comparing with the ^{109}Cd events detected by Pch 3-10 (see Figure 6.23 (right)), we can clearly see that the grade 7 events significantly increase. We think that the increase in the ratio of grade 7 is due to the very thick depletion layer of Pch 5-9. In general, the width of the charge cloud is wider as the depth where X-ray photons are absorbed is deeper. The extent (1-sigma width) of the X-ray event absorbed in the depletion layer is described by the following equation [30];

$$\sigma = \sqrt{\frac{2D\epsilon_{si}}{\mu q N_D} ln(\frac{d_{DL}}{d_{DL} - x})} \ [\mu\text{m}], \tag{6.2}$$

where $D, \epsilon_{si}, N_D, d_{DL}$, and x are the diffusion constant, the dielectric constant of silicon, the densities of the donor, the thickness of the depletion layer, and the absorption depth. Figure 6.21 shows the relationship between the 1-sigma width of a generated charge cloud (σ) and the absorption depth(x) in Pch CCD. Judging from the resistivity, the thickness of the depletion layer of Pch 5-9 is expected to be $\sim$ 300μm. Therefore, based on the relationship shown in Figure 6.21, it is not a surprise even if we detected X-ray events spread 3–4 times wider than those detected by Pch 3-10 (depletion layer 100μm). In the case of this device, we decided to include the grade 7 events in the valid X-ray events (which usually include only grades 0, 2, 3, 4, and 6). We accumulated grade 0, 2, 3, 4, 6, and 7 events and compiled the spectrum of ^{109}Cd. We estimated the count rate of the detected X-rays of ^{109}Cd (mainly 22.2 keV) from this spectrum and found the detection efficiency to be 15.5%

(at 22.2 keV), which exceeds that of Pch 3-10 (6–8%) as expected. This detection efficiency corresponds to that of the ∼260 μm-thickness depletion layer, which is comparable to the thickness of the depletion layer of the Pch CCD developed by LBNL (∼ 300μm)[14].

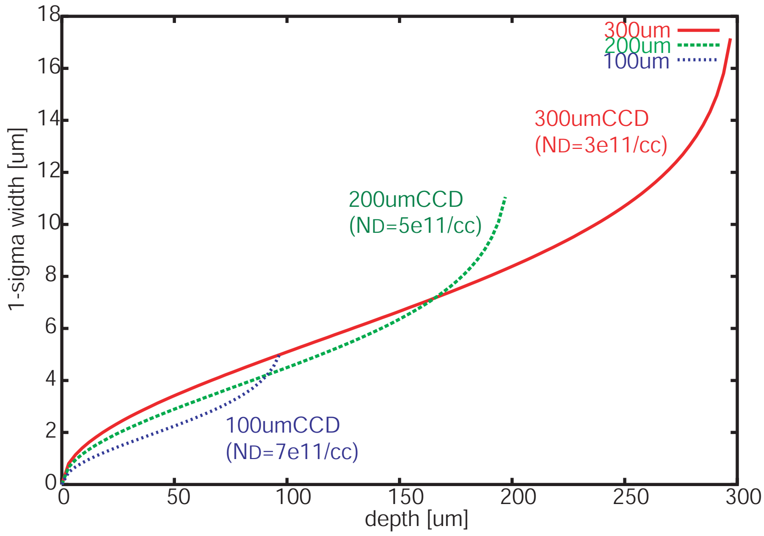


Figure 6.21: Relationship between the width of a generated charge cloud and absorbed depth in Pch CCD.

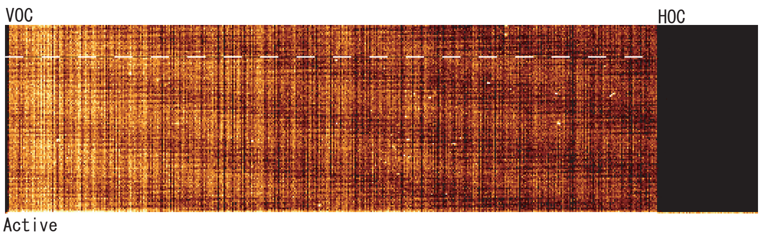


Figure 6.22: Acquired X-ray image of ^{109}Cd with the Pch 5-9. The white dotted line shows the border between the active and VOC regions.

As mentioned previously, when the depletion layer becomes thick, the distance, which the signal carrier (hole) generated in the depletion layer moves to the gate electrode, increases. Therefore, the drift time increases and the hole clouds spread out widely by thermal diffusion before reaching the gate electrode. Because it is difficult to reconstruct the charge of widely spread events, we need to restrain the size of the hole cloud to be as small as possible.

We solve this problem by installing a **back bias** electrode on the backside surface of the Pch CCD. In the case of the ordinary MOS-type CCD, the potential of the backside surface is equal to that of the substrate. By forming a back bias

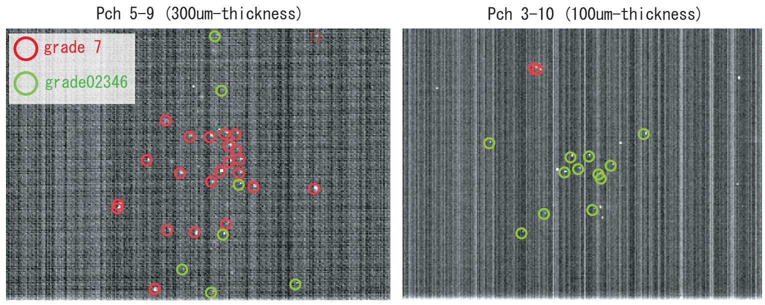


Figure 6.23: Acquired X-ray image with Pch 5-9(left) and Pch 3-10(right). Incident X-rays are from the radio isotope ^{109}Cd (mainly 22.2 keV). The red circle shows grade 7 events spread over 2×2 pixels and the green circle shows grade 0, 2, 3, 4, 6 events, spread within 2×2 pixels.

electrode and applying a reverse voltage (positive for Pch CCD) to it, we increased the potential difference between the front and back side of a wafer. We show the schematic view of the back bias structure in Figure 6.24.

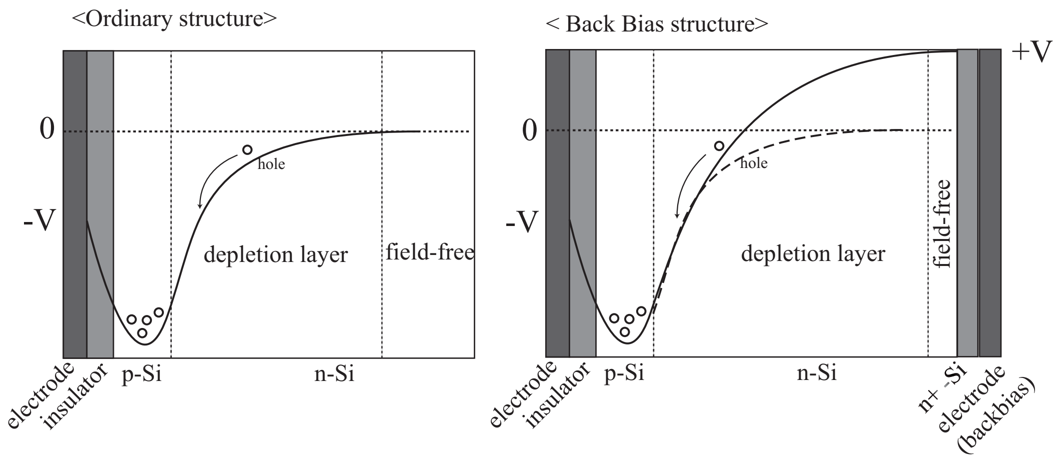


Figure 6.24: Schematic view of the potential well of an ordinary and the back bias structure.

Then, we can reduce the drift time of the holes and restrain the size of the hole cloud to be small as a result, because the electric field in the depletion layer is intensified. Furthermore, there is also another advantage in that we can safely apply a large potential difference which is needed to make the depletion layer wider.

Pch 5-9 is the first test device which is formed a back bias electrode. By applying various voltages of +5, +10, and +15 V to the back bias electrode, we examined (1) whether the size of the charge distribution is really restrained, and (2) whether the detection efficiency improves as we apply the higher voltage to the back bias electrode. This examination was performed using the collimated X-ray source of

^{109}Cd (see section 5.2.1). We show the detection efficiency and the grade branching ratio of ^{109}Cd for various back bias voltages in Table 6.6. In this experiment, we accumulated grade 0, 2, 3, 4, 6, and 7 events and compiled the spectrum of ^{109}Cd. The detection efficiency improves as the back bias voltage becomes higher. The detection efficiency of 16.3% (at a back bias voltage of =15V) corresponds to a 276 μm-thick depletion layer. We can also see that, at a high back bias voltage, the ratio of grade 0 and grade 7 events tends to increase and decrease, respectively.

Table 6.6: Comparison of the efficiency and grade ratio of ^{109}Cd events detected by Pch 5-9 at various back bias voltages

V_{BB} †	P_{eff} ‡	g0	g1	g2	g3	g4	g5	g6	g7
[V]	%				%				
5	10.1	4.4	0.9	3.5	3.5	12	5.3	16	53
10	14.2	4.3	0.7	5.0	4.3	14	5.4	19	47
15	16.3	6.5	0.5	5.6	6.4	15	4.8	18	43

†: Voltage applied to back bias electrode.

‡: Detection efficiency of ^{109}Cd. We reconstructed the spectrum by accumulating grades 0, 2, 3, 4, 6, and 7.

Pch8A Pch 8A-7 is the test device fabricated on the same wafer as Pch 5-9 with new processing conditions optimized based on the experience of the development of Pch 3 and Pch 5.

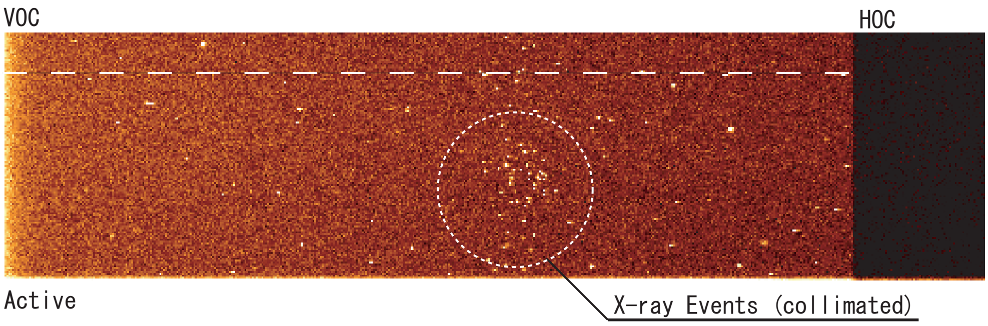


Figure 6.25: Acquired image of ^{109}Cd with Pch 8A-7. The white dotted line shows the border between the active and VOC regions. We irradiated collimated X-rays (^{109}Cd) within the white dotted circle on Pch 8A-7.

Since, as in the case of Pch 5-9, most X-ray events of ^{109}Cd were classified into grade 7, we reconstructed the X-ray events by the fitting method. We found that the detection efficiency of Pch 8A-7 reached 20.2%, which corresponds to a 349μm-thick depletion layer. This detection efficiency seems to be different from that of Pch 5-9. Since the amp gain of Pch 5-9 is smaller than that of Pch 8A-7, the readout noise is high and this may prevent the reconstruction of a part of the ^{109}Cd events. We describe the improvement of the amp gain in section 6.2.4.

Pch14B Pch 14B-5 is the test device formed on the new wafer with the high resistivity (>10 k$\Omega \cdot$ cm). This wafer has a diameter of 6 inches, therefore, the process line is different from than that of test devices described below (Pch3, 4, 5, and 8A). The reason for changing the size of the wafer is discussed in section 6.1.3. This device is also equipped with a guard ring structure so that we can safely apply a high back bias voltage. The guard ring electrode is installed in order to restrain the leakage current. Most leakage current is observed at the edge of the detector as the surface leakage current, therefore, we installed the guard ring electrode around the outside of the CCD. The leakage current is then absorbed in this electrode and we can safely apply a high voltage to the detector.

We applied +12 V and +24 V to the back bias electrode and irradiated collimated X-rays of ^{109}Cd. We found that the detection efficiency is 21.8% and 22.4% respectively for the two back bias voltages, which corresponds to that of the 360 and 372μm-thick depletion layer, respectively. We note that the X-ray events detected by this device at the back bias voltage of +24 V show a horizontal tail which may be caused by a transfer failure. This suggests that we need to adjust the gate transfer voltage with respect to each back bias voltage.

Pch15 Pch 15-14 is one of the final devices among the test devices of Pch CCD. This CCD is fabricated on the high resistivity (10 k$\Omega \cdot$ cm) wafer and thinned to 200 μm. The illumination method for this device is back-illumination. Judging from the high resistivity of the wafer, since the thickness of the depletion layer of this device is expected to be over 200 μm, we can expect that the device is fully depleted by the thinning.

We irradiated collimated X-rays of ^{109}Cd and successfully detected the events as shown in Figure 6.27. We reconstructed the X-ray events by the fitting method and found the detection efficiency for X-rays from ^{109}Cd (22.2 keV) to be $\sim$ 193 μm. This is essentially equal to the thickness of the wafer (200μm) and suggests that this device is probably fully depleted. We describe the characteristics of this device in detail as well as the back illuminated structure in the following section.

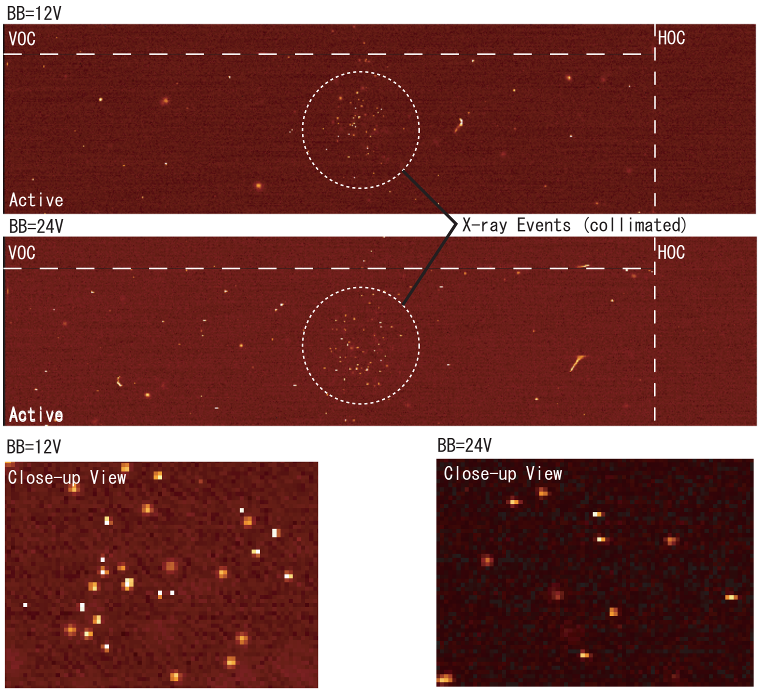


Figure 6.26: Acquired image of X-rays with Pch14B-05. (Upper) The back bias voltage is 12 V. (Middle) The back bias voltage is 24 V. (Bottom) Close-up view of detected X-ray events. Due to its thick depletion depth and large energy of X-rays from ^{109}Cd, most of the X-ray events are spread over 2×2 pixels.

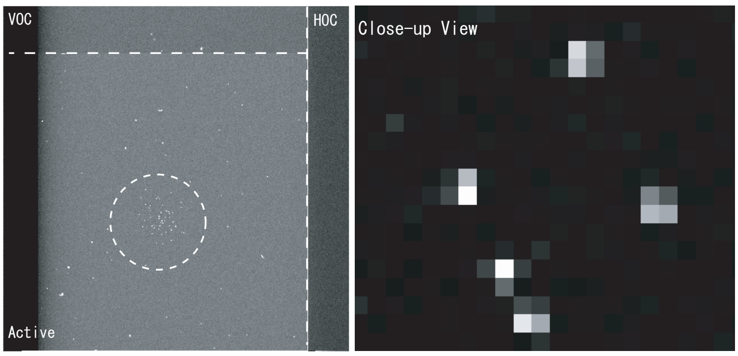


Figure 6.27: Acquired image of X-rays with Pch 15-14. The back bias voltage is 0 V. (left) The white dotted line shows the border between active and VOC, and HOC regions. We irradiated collimated X-rays (^{109}Cd) within the white dotted circle area on this device. (right) Close-up view of detected X-ray events. Due to its thick depletion depth, back-illuminated structure, and large energy of X-rays from ^{109}Cd, many X-ray events are spread over 2×2 pixels and are classified into grade 7.

6.2.3 Improvement of detection efficiency for soft X-rays

As described in the previous section, we confirmed that we can obtain a CCD which has a high sensitivity for hard X-ray photons, by adopting a Pch CCD. We also successfully achieved the thickness of the depletion layer over 300 μm. This makes it easy to remove the field-free region and adopt "a back illuminated structure" in order to increase the quantum efficiency for soft X-rays. As we discovered in the fabrication of Nch BS-CCD, we cannot apply the chemical etching method to the high resistivity wafer. Therefore, we are required to remove the field free layer using the mechanical grinding and polishing methods. From the experience of Nch CCD, we have already confirmed that we can mechanically thin the Si wafer to 150 μm without any mechanical damage or performance degradation, which is independent of the resistivity of the wafer. In the case of Nch CCD, since the depletion layer thickness increases to 80 μm, a field free layer was left $\sim 70\mu$m. On the other hand, since the depletion layer thickness of Pch CCD increases to over 300 μm, we can expect that we can get rid of the field-free layer completely by thinning the wafer down to 300 μm.

In this section, we present the results from the performance evaluation for Pch BI-CCD fabricated on the n-type semiconductor.

6.2.3.1 test device

Table 6.7: Specifications and typical performance of test models of Pch CCD (Back Illumination)

Type No.	Pch 9-17	Pch 15-14	Pch 15-22
Format		512 × 512	
Pixel size		24 μm × 24 μm	
Clock phase		2 phase	
Transfer method		Full Frame Transfer	
Illuminated method		Back Illuminated	
Wafer Resistivity	10k$\Omega \cdot$cm	10k$\Omega \cdot$cm	10k$\Omega \cdot$cm
Depletion layer	-†	193 μm	-†
Wafer⋆	200 μm	200 μm	200 μm
Remarks	-	-	Al coating

†: (not measured.)

⋆: Nominal value reported by HPK (not measured).

Pch9 Pch 9-17 is the first test device of the BI-CCD fabricated on the n-type semiconductor. The resistivity of the wafer is 10k $\Omega \cdot$ cm. The format and package of these devices are different from those of the FI-CCDs described in the previous section. We show an overview of the Pch 9-17 in Figure 6.28 (left).

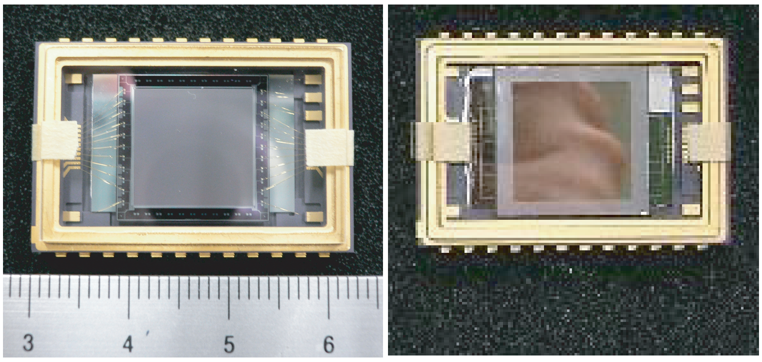


Figure 6.28: A photograph of the back-illuminated Pch CCD. Pixel size is 24μm $\times$ 24μm and format is 512 $\times$ 512 pixels. (Left) Pch 9-17 and Pch 15-14. (Right) Pch 15-22. Due to the presence of the Al coating, the hand of the photographer is reflected on the surface.

The wafer is thinned to 200 μm, judging from the wafer resistivity, and the the depletion layer is expected to increase in thickness to $\sim$ 300μm without thinning. We can thus expect that the wafer is fully depleted after the thinning process. As shown in Figure 6.29, we confirmed that this device successfully detected the X-rays of ^{241}Am. Figure 6.30 (left) shows the spectrum accumulated grade 0, 2, 3, 4, and 6 events. We could not find the two characteristic X-ray lines of 16.9 and 17.8 keV separately, due to the high readout noise of $\sim$ 82 e$^-$, most of which can probably be attributed to the noise of the system. As compared to the ^{241}Am spectrum detected by Nch CCD (P15 14-5B1P-4) which has a depletion layer 65-μm thick (see Figure 6.30 right), we see that the magnitude relationship between the 13.9 keV and 16.9 keV lines is reversed. This means that the hard X-ray sensitivity of Pch 9-17 is higher than that of Nch CCD. We note, however, that it is difficult to evaluate this issue quantitatively due to the very high readout noise which may be caused by the bad condition of the drive circuit.

We also found the phenomenon wherein we could not drive this device normally when we applied a voltage of 13 V or more to the back bias electrode. Figure 6.31 shows the acquired images using Pch 9-17 for various back bias voltages of 5 V, 13 V, and 15 V. In the case of back bias voltages of over 13 V, the OS signal also clearly has an improper shape. We could not find the cause of this unusual behavior. However, the test device of Pch 14B-05, which has a guard ring electrode drives normally even if we apply a voltage of 24 V to the back bias electrode (see previous section). Furthermore, Pch 15-22 which has the same structure as this device also drives normally for the back bias voltage of = 25 V (see section 6.2.5). Therefore, it is highly likely that this phenomenon can be solved by adopting the guard ring electrode and optimizing the manufacturing process at HPK.

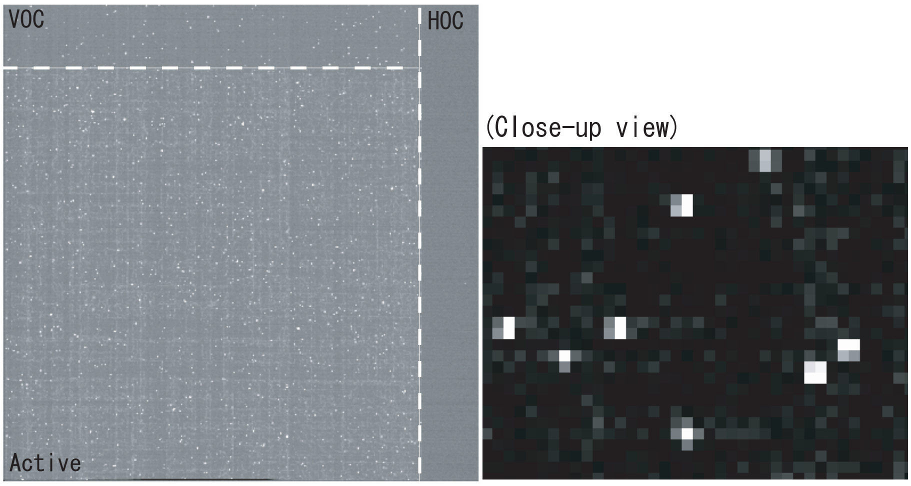


Figure 6.29: Acquired image of ^{241}Am by Pch 9-17 with the back bias voltage of 5V. The white dotted line shows the border between active and VOC, and HOC regions. We irradiated X-rays (^{241}Am) over the whole area of the CCD.

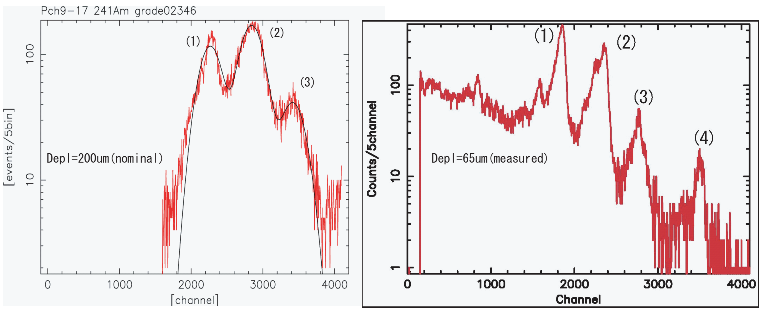


Figure 6.30: (left) Spectrum of ^{241}Am detected by Pch 9-17 with a back bias voltage of 5V. Grade 0, 2, 3, 4, and 6 events have accumulated. (1), (2), (3), and (4) shows the characteristic X-ray lines of 13.9 keV, 16.9&17.8 keV, 20.8 keV. and 26.2 keV, respectively. We successfully detected X-ray events by the back-illuminated and fully-depleted X-ray CCD. However, we could not find the two emission lines of 16.9 and 17.8 keV separately, due to the very high readout noise of ~ 82 e$^-$, most of which can be attributed to the noise of the system. (right) Spectrum of ^{241}Am detected by Nch CCD which has a 65-μm-thick depletion layer. (P15 14-5B1P-4).

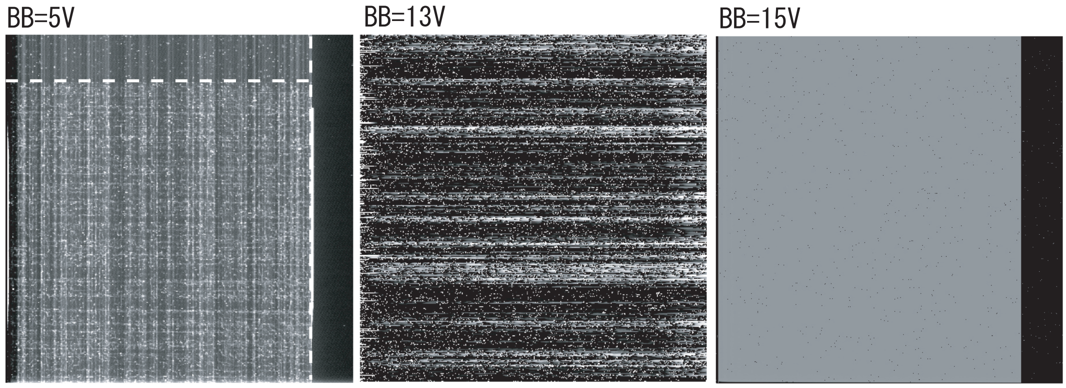


Figure 6.31: Comparison of images acquired by Pch9-17 with various back bias voltage of 5V (left), 13V(center), and 15V(right panel). The white dotted line shows the border between active and VOC, and HOC regions. The exposure time is 1 sec. The dark current is apparently very high. Though the thermometer mounted near the CCD indicated the temperature to be $\sim -90°$C, the CCD device itself may not be refrigerated fully due to problem of the refrigeration setup. When we apply a voltage of 13V or more on the back bias electrode, Pch 9-17 stopped outputting a proper OS signal and we could not acquire normal image from the CCD.

Pch15 As already mentioned in the previous subsection, we confirmed that the BI-CCD of Pch 15-14 successfully detected X-rays and achieved a high detection efficiency for hard X-rays. Figure 6.33 shows the acquired image of β-ray with Pch 15-22. Pch 15-22 is essentially the same as Pch 15-14, except that the surface of Pch 15-22 is coated with Al with a 100 nm-thickness for optical blocking. We irradiated the β-rays (^{90}Sr) over the whole area of the CCD. The energy of the β-rays was 546 keV. A β-ray interacts with silicon with ionization loss and generates electron-hole pairs along its track. The generated charges drift along the electric field in the depletion layer. They create a unique charge distribution whether the charges are generated in the depletion layer or the field-free region. We show a schematic view in Figure 6.32; when a β-ray interacts in the depletion layer, the created holes drift rapidly to the gate electrode, thereby forming a narrow charge distribution of the track as a “tail”. On the other hand, when a β-ray interacts in the field-free layer, the created holes expand slowly by diffusion to reach the depletion layer, thereby forming a wider charge distribution of the track in the form of a “head”. Therefore, if the device is fully depleted, there are no β-ray events which have the “head” structure. As shown in Figure 6.33, we cannot see β-ray events with a “head”, therefore, we can expect that almost the entire field-free region is removed.

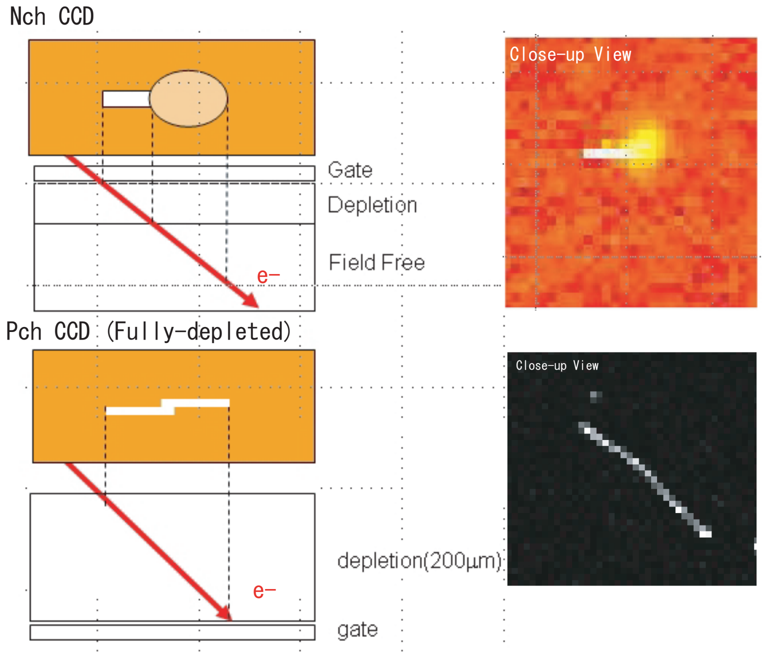


Figure 6.32: Schematic view of the interaction of β-rays in a CCD and the example of the image of the β-ray track obtained by a CCD. (Upper) The case of the typical Nch CCD. The image of β-ray track is obtained by CCD-CREST [64].(lower) The case of the fully-depleted CCD.

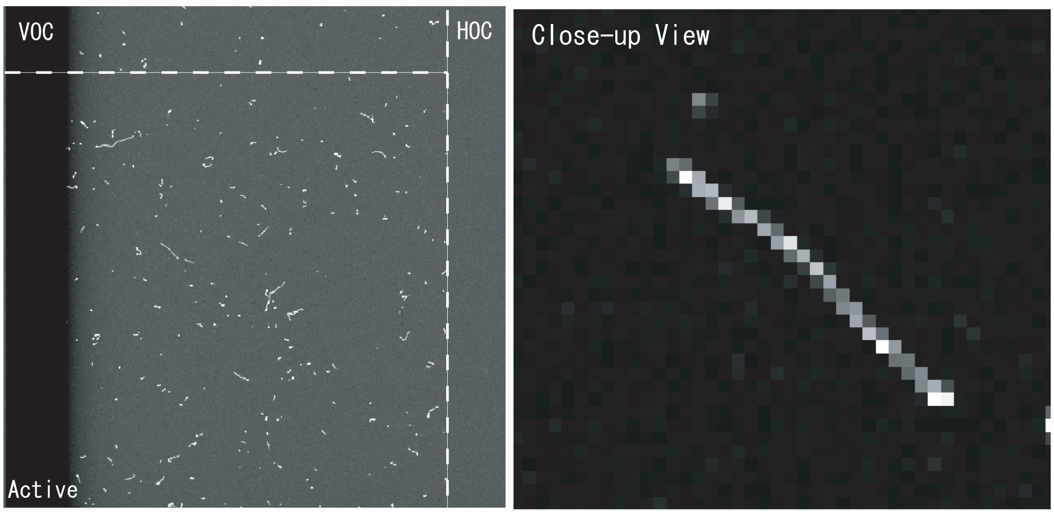


Figure 6.33: Image of β-rays from ^{90}Sr detected by Pch15-22 with a back bias voltage of 5V. The white dotted line shows the border between active and VOC, and HOC regions. We irradiated the β-rays (^{90}Sr) over the whole area of the CCD.

6.2.4 Amp gain and CTI

At the stage of trial production, we found that the test devices of Pch CCD suffer (1) low amplifier gain, and (2) bad CTI as compared with those of Nch CCDs.

These imperfections brought about a degradation of the spectroscopic ability, which is one of the features of a CCD. We solved these problems using the following process.

6.2.4.1 Amp gain

The node sensitivity of Pch 3-10 and Pch 5-9 is 0.8 and 0.9 μV/e$^-$, repectively, which is much smaller than the values for Nch CCDs (about $2-3$ μV/e$^-$,see also Table 6.1). This is because in the layout design of the FDA of these devices, we diverted the existing mask design, which is optimized not for Pch CCD but for Nch CCD. Therefore this small amplifier gain is just as we expected. This problem has been solved by optimization of the FDA design by HPK. The node sensitivity of Pch 8A-7 was improved to 1.6 μV/e$^-$, which is ~ 2 times higher than that for Pch 3-10 and Pch 5-9. Kamata et al. (2004) [27] also reported that the node sensitivity of the test devices of FI8A-I (Pch 8A-2) and FI8A-IV(Pch 8A-7) were improved to 2.2 and 2.0 μV/e$^-$, and their read out noise was 9 and 11 e$^-$, respectively. This value is essentially equivalent to those of the established Nch CCD. As shown in the following subsection 6.2.5, Pch 15-22, which is the final test model of the Pch CCDs also achieved a high node sensitivity of ~ 1.8 μV/e$^-$.

6.2.4.2 CTI

We also had the problem of poor CTI of the Pch CCD. In order to investigate the cause of the poor CTI, we performed the "Fat Zero" experiment. Fat Zero is the technique employed to improve CTI which is attributed to many trap levels. We injected some charges (sacrificial charges) to the whole area of the CCD in advance. Then, trap levels were filled, which allows the signal charge to be transferred without significant loss due to the trap levels. Therefore, if the CTI is significantly improved by Fat Zero, then the main cause of the poor CTI is the existence of many trap levels. Note that this method is, however, rarely adopted for scientific observations, because it has the disadvantage of increasing the shot noise of the sacrificed charge in addition to the readout noise.

We performed this examination using the test device Pch 8A-7. Without Fat Zero, we found the CTI to be 5.2×10^{-4}/transfer (horizontal) and 6.4×10^{-4}/transfer (vertical) which are significantly poorer than those of the Nch CCD (see also Table 6.1).

We installed a red LED in the vacuum chamber in order to irradiate visible light. We evaluated improvements of the CTI with various amounts of optical photons incident on the CCD. We adjusted the amount of optical photons by the length of the luminous time of the LED illumination. We acquired data at luminous times of 0, 2, 4, and 6 sec. The exposure time of the CCD is 10 sec in all cases. Figure 6.34 shows an image acquired by the Pch 8A-7 with 6-sec irradiation of LED light. We show the results in Table 6.8 and in Figure 6.35. It can be clearly seen that the CTI is significantly improved by the Fat Zero method, therefore, we confirmed that a poor CTI mainly causes many trap levels in the Si wafer. Based on these results, we decided to build a test device using wafers supplied by other wafer vendors. Pch 14B-05 is one of the test devices fabricated on the new wafers (see also section 6.2.2). We found that the CTI was significantly improved to be 2.4×10^{-6}/transfer (horizontal) and < 0/transfer (vertical), and reconfirmed that a poor CTI is attributable to the trap levels.

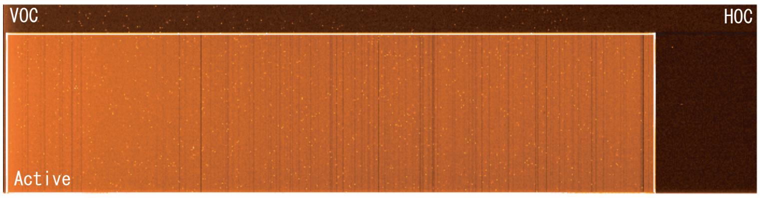


Figure 6.34: Image acquired by Pch 8A-7 with 6-sec irradiation of LED light. We also irradiated X-rays of ^{55}Fe on the whole area of the CCD. The exposure time is 10 sec. The temperature of the CCD is -89 °C

Table 6.8: Relationship between luminous time of LED and CTI of Pch 8A-7

Luminous time [s]	0	2	4	6
Generated Charge[e^-]	45	331	594	874
$CTI_H[10^{-4}$/transfer]	5.2	1.1	0.6	0.9
$CTI_V[10^{-4}$/transfer]	6.4	4.2	3.4	2.5

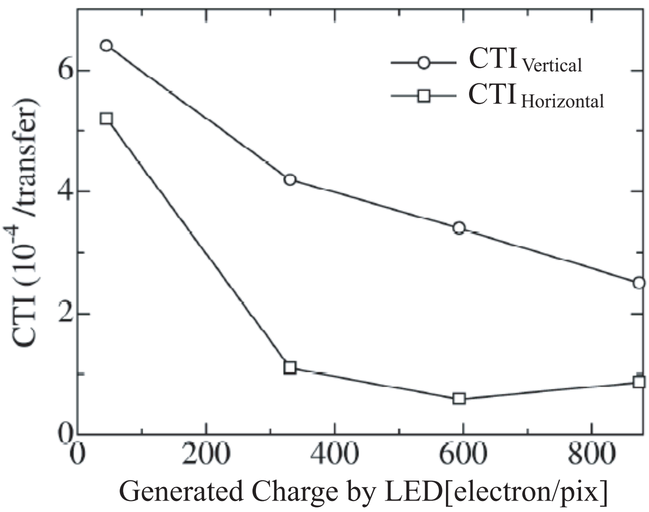


Figure 6.35: Relationship between luminous time of the LED and CTI of Pch 8A-7

6.2.5 Final test device

As shown previously, we identified and solved problems in each development plan through the performance evaluation of test devices of Pch CCD. Based on the results of these developments, the Pch 15-22 was built as a final test device of Pch CCD. We have already mentioned in section 6.2.3 that this device has a wafer with 200-μm thickness and could be fully depleted. Using this device, we performed performance evaluations in order to confirm whether this device maintains the characteristics which we have already achieved in other test devices.

Figure 6.36 shows an image of the X-rays from ^{109}Cd acquired by Pch 15-22 with a back bias voltage of 10V. We irradiated X-rays over the whole area of the CCD and successfully detected them. Table 6.9 shows the characteristics of Pch 15-22 with various back bias voltages of 5, 10, 15, and 20V. It can be clearly seen that there are not few changes in the performance dependent on the back bias voltage. It should be noted that the readout noise of $\sim$ 50 e$^-$ is very high, most of which could be attributed to the noise of the system. Because the node sensitivity of this device (1.7–1.8μV/e$^-$) is equivalent to that of Pch 8A-7 (1.6μV/e$^-$), the readout noise of the CCD itself is estimated to be $\sim$ 10 e$^-$ from the results showing that the Pch 8A-7 recorded a low readout noise of $\sim$ 10 e$^-$ in NAOJ[27].

However, the CTI is rather bad compared to that of Pch14B and Nch CCD. Though we do not yet know the factors for bad CTI, there is the possibility that the CTI could be improved by the optimization of the transfer voltages and the condition. The dark current was not detected significantly in the 20-sec exposure time, which means it is sufficiently low to be used as an X-ray CCD.

Table 6.10 shows the grade branching ratio of ^{109}Cd detected by Pch 15-22 for

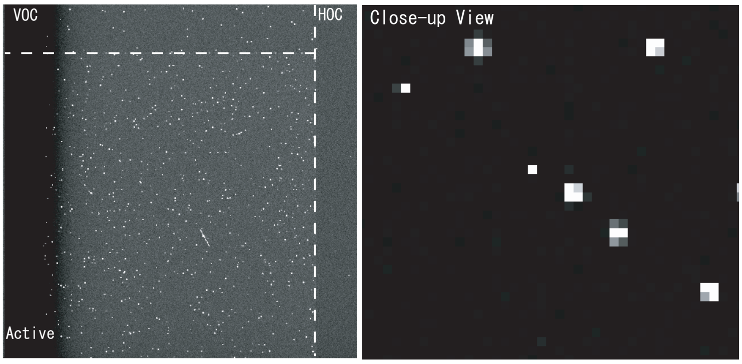


Figure 6.36: Image of X-rays acquired by Pch 15-22 with a back bias voltage of 5V. (left) The white dotted line shows the border between active and VOC, and HOC regions. The exposure time is 18 sec. The temperature of the CCD is -89°C We irradiated X-rays (^{109}Cd) over the whole area of the CCD. (right) A close-up view of the detected X-ray events. Due to its thick depletion depth, the back-illuminated structure, and the large energy of X-rays from ^{109}Cd, many X-ray events are spread over 2 × 2 pixels.

Table 6.9: Comparison of the characteristics of Pch 15-22 for various back bias voltages

$V_{BB}^{\dagger}$	r.o.n‡	$\Delta E^{\star}$	$S_v^{\star\star}$	$CTI_x^{\flat}$	$CTI_y^{\flat\flat}$	$I_{dark}^{\sharp}$
[V]	[e$^-$]	[keV]	[μV/e$^-$]	[10^{-5}/transfer]	[10^{-5}/transfer]	[e$^-$/sec/pix]
5	56	0.95(0.94-0.96)	1.7	5.0(2.0-8.0)	0.95(<3.8)	0(<0.1)
10	54	0.93(0.92-0.94)	1.7	3.9(0.9-6.9)	0(<1.7)	0(<0.1)
15	51	0.83(0.83-0.84)	1.8	2.5(0.44-4.8)	1.3(<3.3)	0(<0.1)
20	54	1.0(0.98-1.0)	1.8	2.0(<4.8)	2.3(< 4.8)	0(<0.1)

Parentheses indicate the 1-sigma confidence limit.

†: Voltage applied to back bias electrode.

‡: Readout noise (r.m.s.).

*: Energy resolution (F.W.H.M.) of ^{109}Cd K_{α} (22.2 keV).

**: Node sensitivity.

$^{\flat,\flat\flat}$: Charge transfer inefficiency of horizontal(x) and vertical(y) transfer.

$^{\sharp}$: Dark current at -90°C.

various back bias voltages. It can be seen that, for a high back bias voltage, the ratio of grade 0 events and grade 7 events tends to increase and decrease, respectively.

Table 6.10: Comparison of grade ratio of ^{109}Cd detected by Pch 15-22 for various back bias voltages

V_{BB}^{a}	g0	g1	g2	g3	g4	g5	g6	g7
[V]				[%]				
5	7.5	0.2	6.8	2.9	2.9	0.5	38	41
10	7.6	0.2	7.5	3.1	3.1	0.8	44	33
15	8.0	0.3	8.3	3.1	3.0	0.8	46	30
20	11	0.1	10.4	5.0	4.3	1.0	51	17

[a]: Voltage applied to the back bias electrode.

We coated the surface of Pch 15-22 with Al to block the optical photons, and we evaluated the efficiency of the optical blocking by the surface Al coating layer. We installed a red LED in the vacuum chamber. We determined the optical transmissivity of Pch 15-22 and compared it with the Pch 15-14 which has no Al layer. Figure 6.37 shows a comparison of images acquired by Pch 15-22 and Pch 15-14. We irradiated light from the LED on to Pch 15-22 and Pch 15-14 at luminous times of 3 sec and 180 msec, respectively. The LED luminance is common in both cases. Nevertheless the luminous time is much longer than that for Pch 15-14. We can clearly see that a small amount of charge is generated in the active area of Pch 15-22. This suggests that the surface Al coating layer successfully blocks optical light, as expected. The amount of generated charge per unit time in Pch 15-22 and Pch 15-14 were 384 e^-/s/pixel and 1.2×10^5 e^-/s/pixel, respectively. Therefore, the transmissivity of the surface Al layer of Pch 15-22 was estimated to be 0.32 %. We note that, however, the transmissivity is possibly overestimated. Since we irradiated LED to the whole area of CCD chip, CCD probably detected LED light incident from the side face of CCD chip which is not coated with Aluminum

6.2.6 Summary of the goal plan

We summarize the development of Pch CCD for SXI following the goal plan as follows.

- Using the high resistivity n-type silicon wafer, we successfully developed the Pch CCDs which have unprecedented high sensitivity for hard X-rays. For example, the test device fabricated on a super high resistivity ($> 10\mathrm{k}\Omega\cdot\mathrm{cm}$) wafer recorded a detection efficiency of over 20% for 22.2 keV, which is significantly higher than that of Nch CCD ($\sim 5\%$).

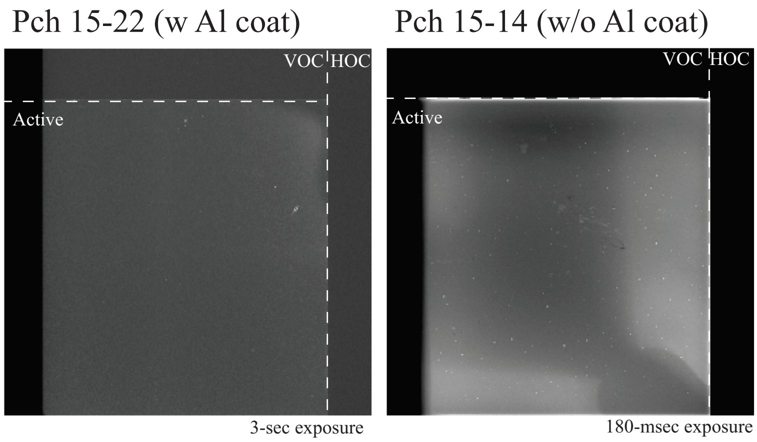


Figure 6.37: Comparison of images acquired by Pch 15-22 (with Al coating) and Pch 15-14 (without Al coating).

- We fabricated the back-illuminated CCD on high resistivity n-type wafer. From the experience of Nch CCD, we safely thinned the wafer to 200μm. We confirmed that this device successfully detected X-rays and was almost fully depleted by the measurement of the detection efficiency for ^{109}Cd and the shape of the β-ray track.

Chapter 7

Development II -Focal Plane Assembly-

In order to reduce the dark current in the exposure time, we need to cool the X-ray CCDs to a low temperature. Furthermore, by cooling the CCD, we can reduce the degree of radiation damage to the CCD in the environment of orbit[41]. We will cool a CCD chip to a temperature of -90 °C using the thermo electric cooler module (TEC) which is assembled with many Peltier devices.

A TEC has already been applied as the main cooling method for X-ray CCDs onboard *ASCA* and *Suzaku*. A TEC consists of multiple semiconductor-based electronic components. When DC power is applied to a TEC, heat moves through the module from one side to the other in proportion to the applied voltage. A TEC can be used either as a cooler or a heater, epending on the direction of current flow Because a TEC uses no moving parts, and employs no fluids, thereby eliminating the need for piping and mechanical compressors used in vapor-cycle cooling systems, it has the advantage of compact and durable. Thus, a TEC is often adopted as the cooler for a CCD carried on a satellite. For efficient use of the limited power resources available onboard a satellite, we need to reduce the power consumption of the TEC to be as low as possible.

A CCD carried on a satellite is usually assembled with the cooling system, including a TEC and associated electronics, in a single unit. We usually call this unit the "Focal Plane Assembly" (FPA). Since they are closely connected to each other, we cannot perform any estimations of the heat budget separately. In this chapter, we describe the design and development of the cooling system and focal plane assembly (FPA) of the SXI.

7.1 Design Concept

In the design of FPA for SXI, we mostly paid attention to reducing the power consumption of cooling. In order to cool down a CCD device efficiently, we need

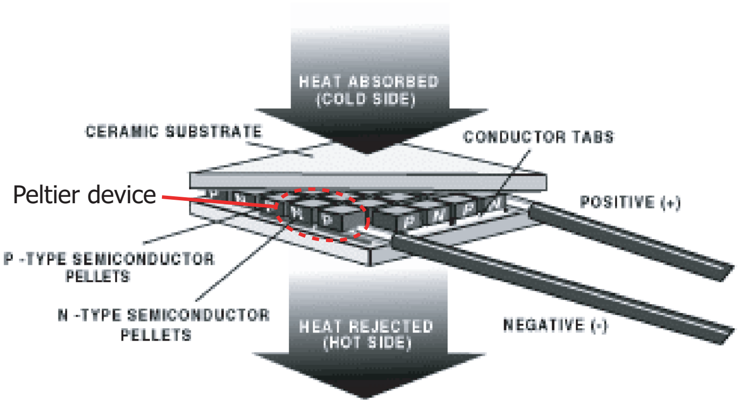


Figure 7.1: Schematic view of an ordinary single-stage TEC module.

to (1) develop a TEC with high performance, and (2) reduce the heat input into a CCD chip. In the following subsection, we describe (1) the development of the TEC for SXI, (2) factors of heat input, and (3) several solutions to reduce the heat input.

7.1.1 Peltier device

A TEC module is assembled with many Peltier devices. We show a schematic view of an ordinary TEC module in Figure 7.1.

In this subsection, we briefly explain the principle of the Peltier device, as basic knowledge for the design of the TEC module.

In 1834, Peltier discovered the inverse of the Seebeck effect, now known as the "Peltier effect". By applying a voltage to thermocouple, a temperature difference is caused between the junctions. This results in a small heat pump, which subsequently came to be known as a "Peltier device".

We show the schematic view of a typical Peltier device in Figure 7.2. The structure of the Peltier device includes π-shaped p-type and n-type semiconductors connected in series. A positive voltage applied to the n-type material drives electrons from the p-type to the n-type material, and heat then moves from the cold side to the hot side (downward in Figure 7.2) by the Peltier effect. The temperature on the cold side decreases as heat is absorbed and that on the hot side increases. The heat budget is given by the following relation;

$$Q_c + pI^2r + k\Delta T = \alpha T_c I \tag{7.1}$$

$$(1-p)I^2r + \alpha T_h I = Q_h + k\Delta T. \tag{7.2}$$

Q_c and Q_h are the net heat absorbed at the cold side and the net heat removed at the hot side, respectively. r and I represent the resistance and the current of the

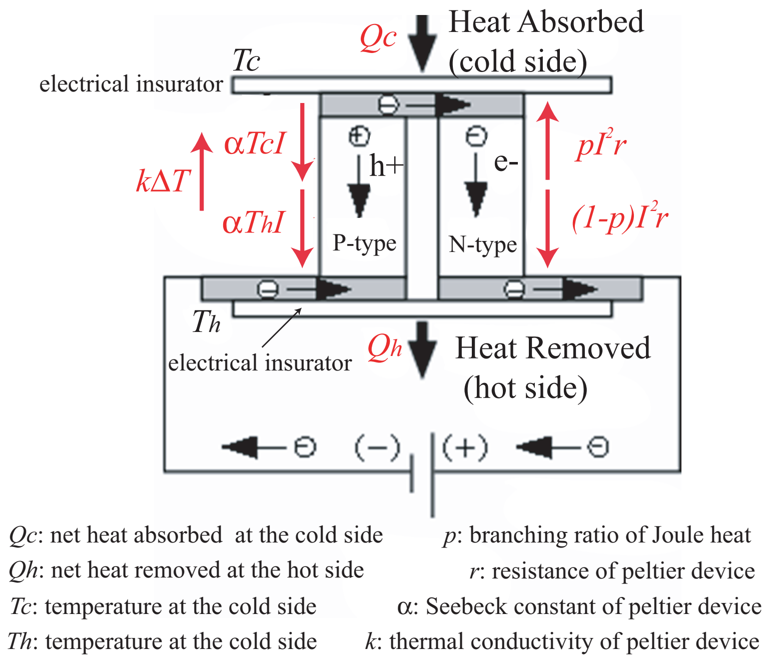


Figure 7.2: Conceptual diagram of a Peltier device.

Peltier device; the Joule heat (I^2r) generated in the Peltier device is conducted to the cold side and the hot side. p is the branching ratio of the Joule heat, which is ordinarily 0.5. k is the thermal conduction coefficient, and the heat of $k\Delta T$ moves upward (from the hot side to the cold side) by thermal conduction. α refers to the Seebeck coefficient of the semiconductor. By the Peltier effect, the heat of $\alpha T_c I$ is absorbed at the cold side and the heat of $\alpha T_h I$ is reduced at the hot side.

From these relations, we found the main factors to determine the characteristics of a Peltier device.

We changed equation 7.1 as follows;

$$Q_c = -\frac{1}{2}(I - \frac{\alpha T_c}{r})^2 + (\frac{\alpha^2 T_c^2}{2\rho} - \kappa\Delta T)(\frac{S}{l}), \tag{7.3}$$

where ρ, κ, S, and l are the resistivity, thermal conductivity, cross section, and length of the semiconductor, respectively.

In order to absorb the heat at the cold side, Q_c must be positive under some conditions, therefore:

$$\frac{\alpha^2 T_c^2}{2\rho} - \kappa\Delta T > 0, \tag{7.4}$$

$$\Delta T < \frac{\alpha^2 T_c^2}{2\rho\kappa}. \tag{7.5}$$

Equation 7.5 shows the maximum difference (ΔT_{max}) in temperature between the cold side and hot side, or

$$\Delta T_{max} = \frac{\alpha^2 T_c^2}{2\rho\kappa}. \tag{7.6}$$

In the case of SXI, we planned that (1) the temperature of CCD be −90 °C (cold side) and (2) the temperature of the heat sink be −45 °C (hot side). Assuming the parameters of typical Bi-Te semiconductors of the Peltier device are equal to those of Peltier device adopted by the TEC of *Suzaku* XIS[48], or

$$\rho = 0.98 \times 10^{-3}\Omega \text{ cm}, \tag{7.7}$$

$$\kappa = 1.65 \times \text{W cm}^{-1} \text{ K}^{-1}, \tag{7.8}$$

$$\text{and} \tag{7.9}$$

$$\alpha = 1.98 \times 10^{-4}\text{V K}^{-1}, \tag{7.10}$$

and $T_c = -90$ °C, then,

$$\Delta T_{max} = 40\text{K}. \tag{7.11}$$

Therefore, a one stage TEC cannot achieve the required difference in temperature of 45 K at $T_c = -90$ °C. By increasing the number of stages of a TEC, the efficiency of cooling of the TEC is improved because the temperature gap per one stage becomes lower. On the other hand, the Peltier device is fragile and a very thin, multi-stage TEC usually requires mechanical support using posts to support the weight. For example, a three-stage TEC used as the cooler in the *Suzaku* XIS needs three posts to support the CCD device (see Figure 7.3 left).

Due to these posts, there is a large heat input to the CCD chip by thermal conduction. As described later (see Table 7.1), the fraction of the heat input attributable to the posts is over 25% of the total heat input. Furthermore, we have the problem that the bottom of the CCD device is separate from the top side of the TEC by thermal cycles, because of the difference of the thermal expansion between the TEC and posts. Though this problem has already been solved by matching the thermal expansion between the TEC and posts by improvements of the TEC and by changing the material of the posts, this problem has the potential to cause degradation of thermal contact and, at worst, destruction of the TEC by bending and/or shear stress.

On the other hand, in the case of MAXI-CCD, the CCD chip is directly glued to the top of the TEC and is supported only by the TEC itself, *i.e.* not by posts (see Figure 7.3 right), so that the heat input caused by thermal conduction can be minimized. In order to reduce the weight of the CCD, (1) the package structure in which a CCD chip is usually installed is removed, and (2) the CCD chip is connected

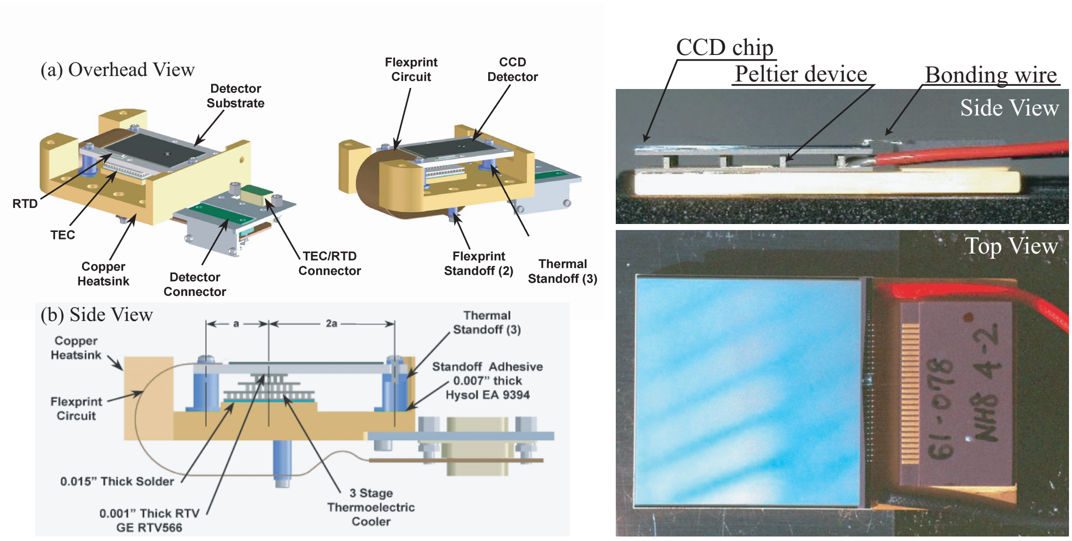


Figure 7.3: (left) Schematic view of FPA of *Suzaku* XIS. The CCD device is supported by a 3-stage TEC and three standoffs (posts). (right) Picture of MAXI-CCD. To reduce the heat input to the CCD as much as possible, a unique structure is used.

via bonding wires to the hot side instead of a flexible printed circuit. Since the bonding wire is aluminum wire which is thin (20-μm diameter) and short (3 mm), this is significantly lighter than a flexible printed circuit. Because the temperature of a CCD chip is -60 °C, which is a relatively high temperature, and the difference in temperature between the CCD chip and heat sink is 40 K which is relatively small, such thermal conditions can be realized by a single-stage TEC.

In the case of SXI, however, the temperature difference of 45 K between the CCD chip and the heat sink is too large to be achieved using a single-stage TEC, as shown in equation 7.11. We therefore designed the FPA consisting of a 2-stage TEC without posts. We have examined the possibility of realizing such a unique structure in cooperation with HPK and Aisin Seiki Co. Ltd. (AISIN).

7.1.2 Heat budget

In this subsection, we estimate the heat input to a CCD chip and introduce our design plan to reduce the heat input as much as possible.

Wire bonding In order to sustain a CCD device with only the TEC module, we need to reduce the mass of the CCD chip as much as possible. In the case of XIS, as shown in Figure 7.3 (left), the CCD is wired by a flex print circuit. However, because the flex print circuit is very heavy, it is expected to be difficult to support only with the TEC. Based on the experience with MAXI-CCD, we decided to adopt wire bonding for the electrical connection between a CCD chip and the hot side.

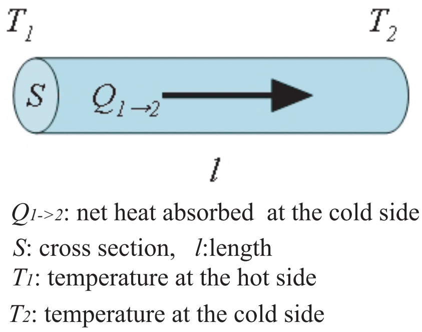


Figure 7.4: Conceptual diagram of heat transfer due to thermal conduction.

On the other hand, since the wires, which distribute the clock voltage for driving the CCD, connect the hot side to the CCD (cold side), this is one of the main paths of heat input. We need to study the heat input through these wires. Assuming the thermal condition shown in Figure 7.4, the heat transfer $Q_{\rm cond}$ through the wires is the following equation of heat conduction;

$$Q_{\rm cond} = \rho \frac{S}{l}(T_1 - T_2), \tag{7.12}$$

where ρ, S, l, T_1, and T_2 are the coefficient of thermal conductivity, a cross section, length, temperature at the side of 1, and temperature at the side of 2.

Therefore, to reduce the heat input by the heat conduction, we need to design the bonding wire, paying attention to the following points;

- the material with low thermal conductivity coefficient,
- thin and long wire, as much as possible.

Though Au and Al wires are usually used for the bonding wire, the thermal conductivity coefficient of Al (238 $\mathrm{Wm^{-1}K^{-1}}$) is significantly lower than that of Au (320 $\mathrm{Wm^{-1}K^{-1}}$). Therefore, we decided to use the Al wire. From the view point of mechanical strength and tight bonding, the diameter of the Al wire is limited to 20 mm and the length is up to 3 mm. We note that the specification of this wire is the same as that of the MAXI-CCD. Therefore, we can expect that bonding processing using this wire has already been established. The heat input is 1.0 mW per wire, which is calculated on the assumption that the difference in temperature between a CCD cold side and hot side is 45 K.

Al coating The thermal radiation of the housing of SXI is also the main path of the heat input to a CCD. Since the temperature of the housing is planned to be $\sim -45\,^\circ$C, which is much higher than that of a CCD ($-90\,^\circ$C), the heat input due to

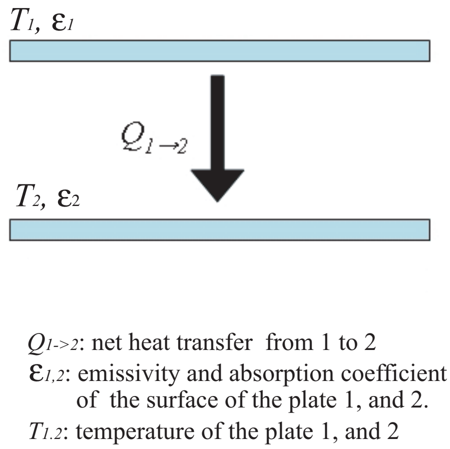


Figure 7.5: Conceptual diagram of the heat transfer due to thermal radiation.

thermal radiation is not negligible. To reduce this heat input, it is effective to coat the surface of a CCD and the housing with the material which has low emissivity and absorption coefficient. This is also evident from the following equation for the heat transfer by radiation (this equation assumes the thermal condition shown in Figure 7.5);

$$Q_{\rm rad} = S\sigma\frac{T_1^4 - T_2^4}{\frac{1}{\epsilon_1} + \frac{1}{\epsilon_2} - 1}, \tag{7.13}$$

where S, σ, T_1, T_2, ϵ_1, and ϵ_2 is the surface area of a CCD, Stefan-Boltzmann coefficient, temperature of plate 1 (assuming the housing), temperature of plate 2 (assuming the CCD), emissivity and absorption coefficient of plate 1, and emissivity and absorption coefficient of plate 2.

The emissivity of the CCD surface is usually ~ 1. On the other hand, aluminum evaporation on the surface of the CCD improves ϵ to 0.1, therefore we can expect that the heat input to the CCD by radiation significantly decreases. As shown in Table 7.1, the heat input by the radiation of MAXI-CCD (15 mW) is smaller than that of *Suzaku* XIS (136 mW). This is because the aluminum is evaporated not on the surface of *Suzaku* XIS but on that of MAXI-CCD. We note that aluminum evaporation plays the role of a filter for optical blocking and is useful to simplify the structure of the housing of a CCD because we need no longer assemble an additional optical blocking filter.

Assuming that we coat the surface of the CCD chip and the housing with the aluminum, we can calculate the heat input to the CCD chip by radiation. We assume that (1) the size of the CCD chip is $75 \times 50\text{mm}^2$ and (2) the CCD chip is enclosed in an isothermal box of -45 °C temperature which corresponds to the housing. Then, the heat input is 27 mW, which is also quite small compared to that of the *Suzaku*

XIS (136 mW)

We summarize the estimated heat inputs to a CCD chip for SXI, comparing the values with those of *Suzaku* XIS and MAXI-CCD, in Table 7.1. Assuming the number of readout nodes and wires of SXI to be 8 and 110, amp heating and conduction heating through the wires is estimated to be 40 mW and 110 mW, respectively. Then, the total heat input is 177 mW. Despite the larger size compared to the *Suzaku* XIS, the total heat input is successfully restrained below that of the *Suzaku* XIS.

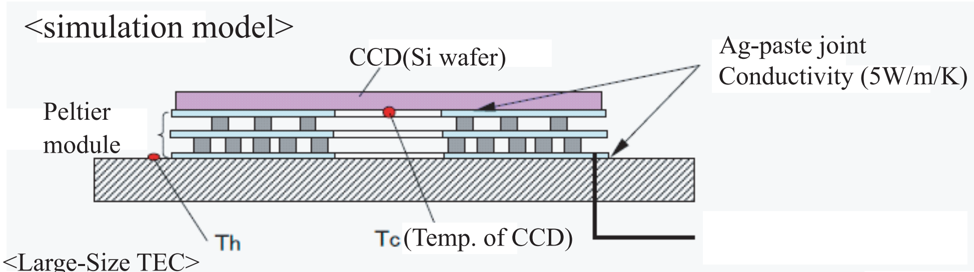
Table 7.1: Comparison with FPAs of existing missions and NeXT-SXI

	Suzaku XIS	MAXI-CCD	NeXT-SXI
Basic Characteristics			
Size of IA	$25 \times 25\text{mm}^2$	$25 \times 25\text{mm}^2$	$50 \times 50\text{mm}^2$
No. of nodes	4	1	8
No. of cables	57	26	110
CCD surface coating	none	Al	Al
Temp. of CCD	-90°C	-60°C	-90°C
ΔT	50K	40K	45K
Heat Input			
Radiation heating	136 mW	15 mW	27 mW
Amp heating	18 mW	2 mW	40 mW
Conduction heating			
from cable	28.5 mW	26 mW	110 mW
from support posts	67.5 mW	0 mW	0 mW
Total heat input	250 mW	43 mW	177 mW
Characteristics of TEC			
No. of stage	3	1	2
Power consumption	4.0 W	1.0 W	7.0 W

7.2 Trial production of TEC module

Based on the calculation results, we designed a TEC with a 2-stage Peltier module, in cooperation with HPK and AISIN. In the design, we established the following goals;

- to sustain a CCD chip of 75mm × 50mm × 300μm without additional posts,
- to absorb heat of 180 mW at the cold side,
- to realize a temperature difference of 45 K between the cold side (T_c) and the hot side (T_h) at T_h is -45°C,



<Large-Size TEC>

Stage(plate)	Size		Height	remarks
Upper	51mm	76mm	5. 77mm (total)	ϕ35 hole
Middle	51mm	76mm		ϕ36 hole
Bottom	52mm*2	76mm		

<Small-Size TEC>

Stage(plate)	Size		Height	remarks
Upper	49mm	20mm	5. 77mm (total)	
Middle	50mm	20mm		
Bottom	50mm	20mm		

Figure 7.6: Simulation model for the heat performance of TEC.

and

- to make a hole of 35 mm-diameter to pass through the hard X-ray penetrated a CCD (back supportless structure).

Large Size TEC First, we planned to build a large-size TEC module (large-size TEC), with a sufficiently large (75mm $\times$ 50mm) stage to load a CCD chip without protruding. The material of the plates for the stage is aluminum nitride (AlN) which has a similar coefficient of thermal expansion as that of silicon. We adopted an AlN plate to reduce the risk of destruction due to the difference in thermal expansion between the CCD and plate caused by the rapid temperature change in cooling. Under the simulation model shown in Figure 7.6, we found that (1) we needed 18 and 81 Peltier devices in the upper and lower stages in order to meet the goals of the TEC, and then (2) we can reach a temperature difference of 45 K with a power consumption of $\sim$ 5 W as a result of the simulation of the heat performance of TEC performed by AISIN. The results are shown in Figure 7.7.

Though the heat input to the SXI is restrained to be lower than that of XIS, the TEC power consumption of 5 W is slightly higher than that of XIS (4.0 W). This is due to the difference in the number of stages. As described previously, with increasing number of stages of the TEC, the efficiency of cooling of the TEC improves because the temperature gap of each Peltier device becomes lower. We found that this TEC has good anti-shock strength, equivalent to that of the MAXI-CCD, as a result of analysis for the mechanical strength by the finite element method

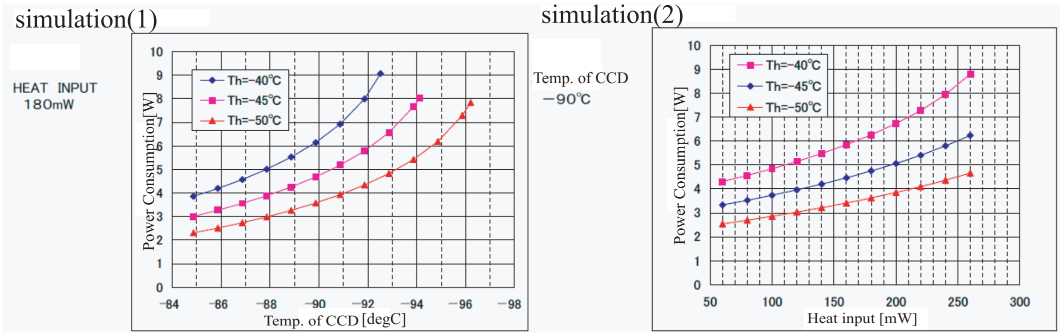


Figure 7.7: Result of simulation for cooling performance of the large-size TEC. (left) Relationship between the temperature of the CCD and the total power consumption of the TEC. The absorbed heat is fixed to be 180 mW. (right) Relationship between the absorbed heat and the total power consumption of the TEC. The temperature of the cold side (CCD) is fixed to be −90°C.

(FEM). Since the MAXI-CCD has already been confirmed to have sufficient mechanical strength to pass the vibration and shock test to simulate a rocket launch, the mechanical strength of this TEC is promising without any additional mechanical support.

On the other hand we had a problem in building up the TEC module. Since we attached the Peltier devices to an AlN plate by soldering, the rapid heating and cooling by soldering makes them deform. Due to the large size of the AlN plate, serious distortion of the AlN plate causes the destruction of the TEC modules. We could not solve this problem though we tried to adopt a low temperature solder and to change the assembling process. We thought that the large size of the TEC itself is the main cause of this trouble, and we decided to divide the TEC into two modules.

Small size TEC We designed a small size TEC, which has a 49mm $\times$ 20mm stage. We planned to support the CCD chip using 2 modules. We also adopted a thick (0.635 mm) AlN plate for the stage in order to reduce the distortion by thermal stress to the stage. The simulation of the thermoelectric characteristics of this TEC was performed under the simulation model shown in Figure 7.6. We found 19 and 41 Peltier devices are necessary, to be attached to the upper and lower stages, in order to meet the goals of thte TEC. Figure 7.8 (left) shows the relationship between a CCD temperature and the total power consumption of the TEC as a result of the simulation. Each TEC module needs to absorb half of the heat input to a CCD chip, therefore, we fixed the heat input of this TEC to 100 mW. We determined a power consumption of $\sim$ 3.5 W per one TEC in order to realize the temperature gap of 45 K. Figure 7.8 (right) shows the relationship between the heat input and the total power consumption of the TEC. Therefore the total power consumption

Table 7.2: Contests of the screening test performed in AISIN

item	exam. condition	acceptance criterion
Thermal cycle	-40°C/-85°C, 15min×20 cycle	(1)internal resistance change is $< 2\%$
Annealing	100°C, 1 hour	(2) internal resistance is 1.01–1.55Ω (upper step) and 1.28–1.80Ω (lower step)
Visual inspection	Microscope ×20	–

is 7.0 W, which is slightly increased compared to the large size TEC. The power consumption of the TEC is, however, still restrained to be only 2 times higher than that of XIS, even though the area of the imaging region of the SXI is 4 times larger than that of the XIS.

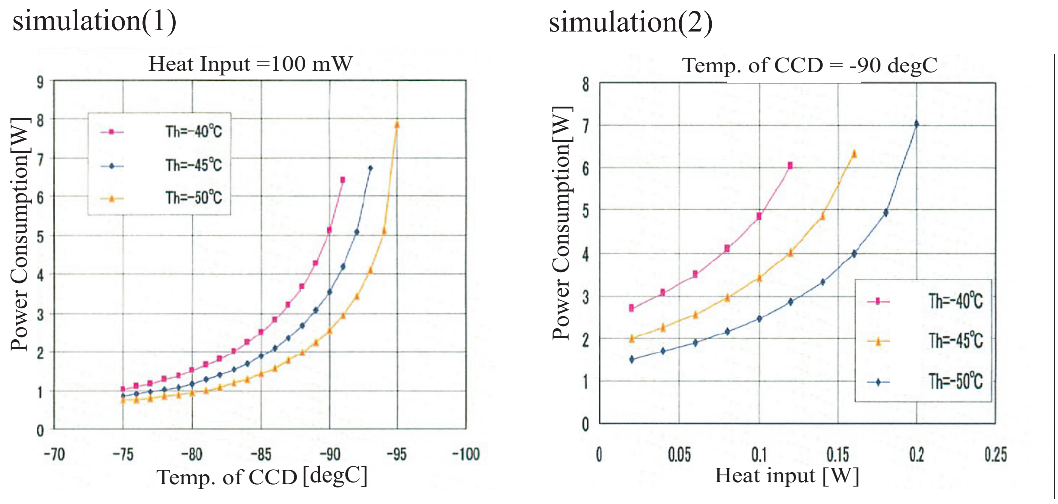


Figure 7.8: Result of simulation for cooling performance of small-size TEC. (left) Relationship between the temperature of the CCD and the total power consumption of TEC. The absorbed heat is fixed to be 100 mW. (right) Relationship between the absorbed heat and the total power consumption of TEC. The temperature of the cold side (CCD) is fixed to be -90°C.

In this design of a small size TEC, the TEC module was successfully assembled without any failures. Figure 7.9 shows the appearance of the small size TEC module. By the screening test performed at AISIN before shipping, this module has already confirmed that the expected electrical characteristics are achieved for the criteria shown in Table 7.2.

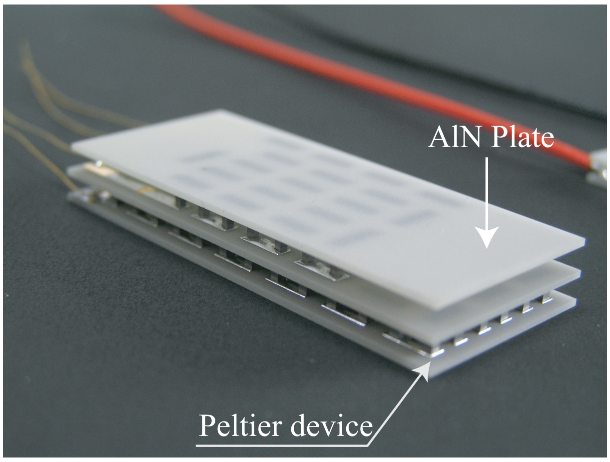


Figure 7.9: Photo of the trial production of the 2-stage TEC module.

7.3 Thermo-mechanical model of FPA for SXI

In parallel to the trial production of the TEC module, we also proceeded with the design of the thermo-mechanical model of FPA for SXI. The purpose of the trial production of the thermo-mechanical model is to examine whether (1) the cooling performance and (2) anti-vibration shock strength were achieved as expected.

We assembled the thermo-mechanical model in a form as similar as possible to the FPA, which will actually be assembled as the device onboard the NeXT satellite. Figure 7.10 shows a drawing of the thermo-mechanical model of SXI-FPA. This model mainly consists of the following parts;

- the trial production of the TEC module (small-size TEC),
- dummy CCD fabricated from AlN,
- Tungsten-copper (CuW) base plate to attach the TEC module,
- Aluminum bonding wires of 20 mm-diameter and 3 mm-length.

The reason why we adopted AlN to a dummy CCD is (1) the thermal characteristics are very similar to that of silicon, and (2) processing of the AlN is easier than silicon. The tungsten copper alloy is suitable for the base plate because of its high thermal conductivity (193W $\mathrm{m^{-1}\ K^{-1}}$) and low thermal expansion coefficient ($6 \times 10^{-6}\mathrm{K^{-1}}$). We note that the thermal expansion coefficient of AlN of $\sim 5 \times 10^{-6}\mathrm{K^{-1}}$ is almost equal to that of CuW. Though Aluminum and Stainless steel (SUS) show good thermal conductivity and are easier to procure and process, their thermal expansion coefficients are $23\times10^{-6}\mathrm{K^{-1}}$ and $15\times10^{-6}\mathrm{K^{-1}}$, respectively. To avoid the risk of destruction due to the difference in the thermal expansion, as

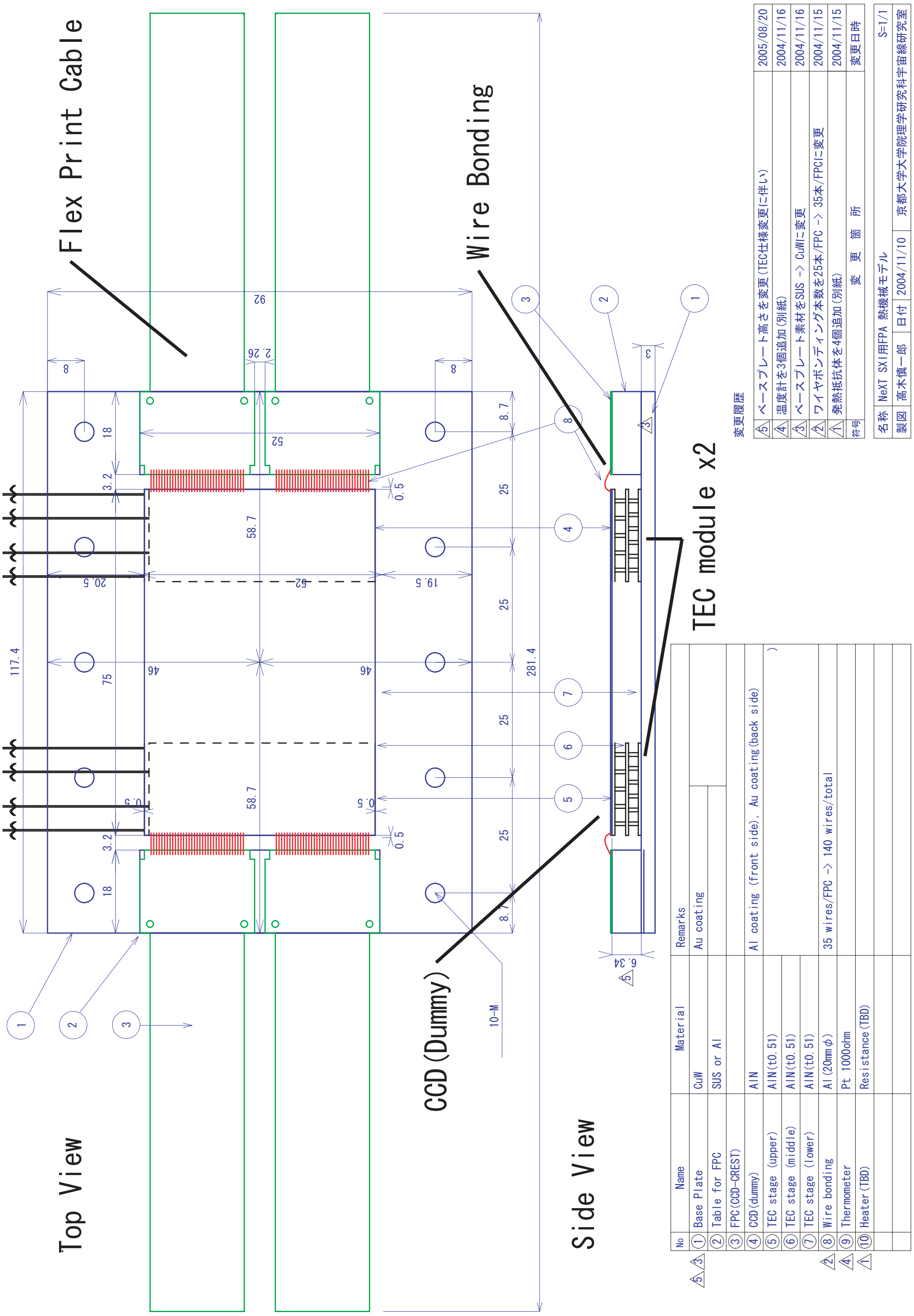


Figure 7.10: Design drawing of the mechanical model of FPA for SXI.

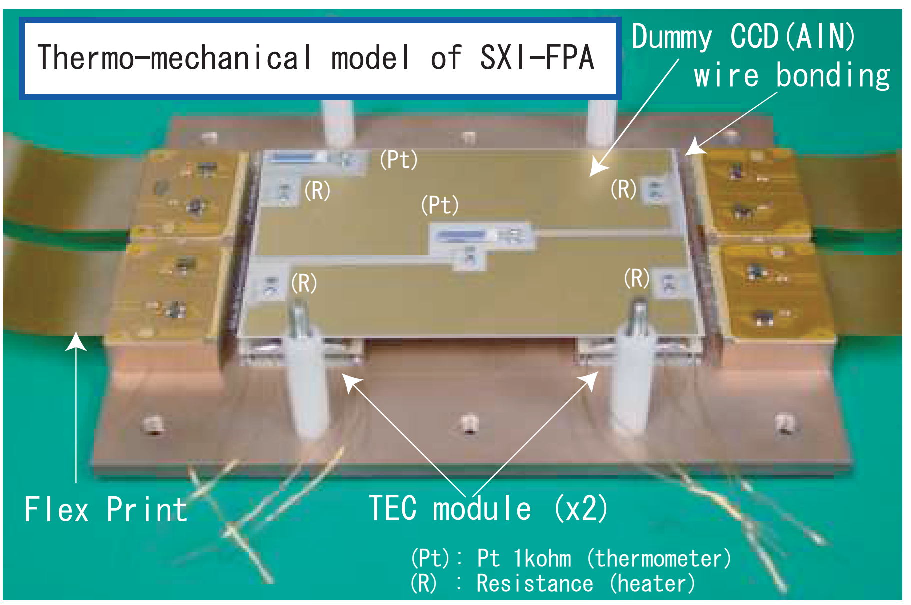


Figure 7.11: A photo of the trial production of the thermo-mechanical model of FPA for SXI.

much as possible, we decided to adopt the CuW alloy as the base plate. To simulate the heat input caused by thermal conduction, we bonded the 140 wires between a dummy CCD and flexible printed cable (hot side). We also attached thermometers of Pt 1kΩ and resistances on the dummy CCD, in order to measure the temperature of the surface and to simulate the heating of the load resistance of the readout FET on a CCD, respectively. They are electrically interfaced through the bonding wires and flexible print cable with the outside.

This model has already been assembled at HPK. A picture of the trial production of this model is shown in Figure 7.11. However, in the inspection performed at HPK before shipping, we found a problem in that the internal resistance of the TEC suddenly increased by the thermal cycle test. Since we have already confirmed that the TEC module itself is driven normally, we considered that the structure of the thermo-mechanical model caused this problem. At present, checking and modification of the structure and assembling process of this model are in progress to solve this problem.

Chapter 8

Summary

Soft X-ray Imager The Soft X-ray Imager (SXI) is the key detector to realize a Wideband X-ray Imager (WXI), which is one of the focal plane detectors of $NeXT$. SXI is required to perform precise imaging and spectroscopic observations in the energy band of 0.5–20keV. From the view point that the X-ray CCD is equipped with high spatial and energy resolutions, the X-ray CCD is the most suitable detector for SXI. On the other hand, the X-ray CCD is required to maintain a high detection efficiency for X-rays in the high energy band, while allowing hard X-rays undetected by the CCD to pass through in order to enter the HXI. To satisfy these requirements, we decided to design and develop the "Back Supportless CCD (BS-CCD)", which has a thick depletion layer, a thin field-free layer, and no package at the rear side. In order to develop the BS-CCD gradually and safely, we developed a "Baseline plan" and a "Goal plan". The former is a rather conservative plan based on the established method to fabricate Nch CCDs, and the latter is an innovative plan which aims to fabricate a Pch CCD.

Back Supportless CCD We fabricated a test model of the BS-CCD using Nch CCD (Nch BS-CCD). The test model of the BS-CCD of P15 14-5B1P achieved excellent performance of readout noise of 7 e^- and energy resolution of 144 eV, which are essentially equivalent to those of the established X-ray CCDs. The thickness of the depletion layer is ~ 70 μm, meaning that this device has one of the most sensitive X-ray detectors for hard X-rays among past and present established X-ray CCDs. We successfully thinned the field-free layer of this device without any performance degradation and confirmed that the thickness of wafer was ~ 190 μm, in accordance with our design. Through the subsequent development of the BS-CCD, we could safely thin down the wafer to 150 μm. Based on these successful results of the test model, we built a medium-size BS-CCD (CCD-NeXT1) in order to confirm the specifications and equipment with the aim of loading it onboard the satellite. CCD-NeXT1 was also successfully driven and achieved excellent performance including (1) low dark current of 12 $e^-s^{-1}pix^{-1}$, (2) thick depletion layer of 84 μm, (3) high node sensitivity of 3.2 μV/e$^-$, and (4) low CTI of $\sim 1 \times 10^{-6}$/transfer. The readout noise of 21 e$^-$ seems to be worse than that of the test device (7 e$^-$), which is attributed to the difference in the CCD driver system. The node sensitivity of CCD-NeXT1 (3.2 μV/e$^-$) is somewhat higher than that of the test devices ($\sim$ 2 μV/e$^-$), therefore the read out noise of the CCD-NeXT1 itself is expected to be equal to or better than that of the test devices.

In parallel with the development of the Nch BS-CCD, we participated in the development of the Pch CCD which is being undertaken by a group of at the National Observatory of Japan (NAOJ). We evaluated the performance of the Pch CCD and confirmed that the thickness of the depletion layer reached over 300 μm, which is $\sim$ 4 times thicker than that of established CCDs ($\sim$ 80 μm). This thick depletion layer suggests that the detection efficiency of hard X-rays is significantly increased. For example, the detection efficiency for 22.2-keV X-rays increased from $\sim$ 5 % to $\sim$ 20 % by increasing the thickness of the depletion layer from $\sim$ 80 μm to $\sim$ 300μm. Such a thick depletion layer allows for the fabrication of the back-illuminated CCD (BI-CCD). We fabricated the test model of the BI-CCD using a wafer thinned down to 200μm. We confirmed that this device was driven normally and obtained results which suggest that a field-free region is no longer left by the measurement of the depletion layer thickness and irradiation of β-rays. Furthermore, through our experiments to improve the performance, Pch CCD achieved excellent performance. (1) We found the problem of low amp gain of $< 1\mu$/V$^-$ in the earlier test device of Pch CCD . This problem was solved by the optimization of the amp structure by HPK, and we confirmed that the amp improved to $\sim 2\mu$/V$^-$, which is comparable to that of Nch CCDs. (2) We also found the problem of poor CTI ($\sim 5 \times 10^{-4}$ /transfer) in the test device of the Pch CCD. Through the Fat Zero experiment, we found the major cause of the poor CTI to be many trap levels in the Si wafer. The new test device was fabricated on a new wafer which was obtained from a different wafer vendor, and we found that this device shows good CTI performance of $< 5 \times 10^{-6}$ /transfer. Finally, we successfully developed the final test device of Pch CCD, which is a BI-CCD and has a $\sim$ 200 μm-thick depletion layer. The readout noise expected from the node sensitivity is $\sim$ 10 e$^-$, which is comparable to that of Nch CCD. The CTI is rather worse ($\sim 2 \times 10^{-5}$ /transfer) than that recorded by Pch 14B. Though there is the possibility that soptimization of the transferring voltage could improve the CTI, we need to continue to investigate this problem . Excluding this CTI problem, Pch CCD is a very promising device for BS-CCD.

Focal Plane Assembly We designed and developed the focal plane assembly (FPA) for SXI. To efficiently cool a CCD chip equipped in the SXI, we are required to reduce the heat input as much as possible. We examined the paths of the heat input and contrived various schemes to reduce the heat input; We designed a new-type of thermo electrical cooler (TEC) which consists of a 2-stage Peltier module and no additional posts, to generate a wide temperature gap of 45 K and to eliminate heat input by thermal conduction through the posts. The thermal radiation of the housing of SXI is also the principle path of the heat input. We found that the heat input by thermal radiation was significantly reduced by the metal coating on the surface of the CCD chip and the housing. In the results, although the size of the imaging area of a CCD chip for SXI is 4 times larger than that of the *Suzaku* XIS, we successfully restrained the heat input to 177 mW, which is much smaller than that of the XIS (250 mW). The power consumption is expected to be 7.0 W, which is only 2 times larger than that of XIS.

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